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# VLSI BASED LOW POWER FRACTIONAL-N PHASE LOCKED LOOP FREQUENCY SYNTHESIZER FOR BLUETOOTH

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## Abstract

Power is the amount to function or generating or shelling out energy. This means that, it is a way of measuring how fast a function can be carried out. So power has become one of the most important parameter in various communication systems such as optical data links, wireless products, microprocessor & ASIC/SOC designs. This paper presents the design and simulation of VLSI based low power fractional- N Phase locked loop frequency synthesizer for Bluetooth application. This phase locked loop is designed using VLSI technology, which in turn offers high speed performance at low power. For improving the performance of fractional-N phase locked loop, Loop filter and Sigma-Delta modulator are the most important factors. The loop filter bandwidth limits the speed of switching time between the synthesized frequencies. The Periodic operation of dual modulus divider introduces phase noise in the PLL. To eliminate this phase noise, the digital Sigma-Delta modulator is used which generates a random integer number with an average equal to desired fractional ratio and pushes the spurious contents to higher frequencies.

**INTRODUCTION**

Phase lock loop is an electronic circuit that controls an oscillator so that it maintains a constant phase angle (i.e. lock) on the frequency of an input or reference signal. It is a control system that generates an output signal whose phase is related to the phase of an input "reference" signal. It is an electronic circuit consisting of a variable frequency oscillator and a phase detector. This circuit compares the phase of the input signal with the phase of the signal derived from its output oscillator and adjusts the frequency of its oscillator to keep the phases matched. A phase locked loop (PLL) can be divided into two architectures, an integer-N PLL and a fractional-N PLL.The fractional-N PLL solves the trade-off issue between channel spacing and loop bandwidth found in the integer-N PLL, offering a lower phase noise, higher frequency resolution and a larger loop bandwidth. The output frequency of the fractional-N PLL is fout = (N.α)* Fref , where N is an integer, and α is the fractional part.A dual modulus divider is used to average many integer divider cycles over time to obtainthe desired fractional division ratio.The main problem of this method is that by using the dual modulus divider periodically generates a spurious tones that is called fractional spur. The best method to remove the fractional spurs is using a Sigma-Delta Modulation technique. Basic PLL is a feedback system composed of three elements: a phase detector, a loop filter and a voltage controlled oscillator (VCO) as shown in figure 1.

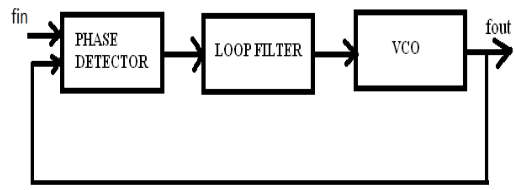


**Figure 1. Block Diagram of PLL**

Three components are connected as a feedback system. The reference signal is periodic such as square wave which is compared with the output of VCO using a phase detector. The output of phase detector is then applied to the low pass filter and used as a control signal to drive a VCO. The VCO will lock onto the reference signal thus can be used to tracked a periodic signal as its phase and frequency varies.

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The electronics industry has achieved a phenomenal growth over the last two decades, mainly due to the rapid advances in integration technologies. The number of applications of integrated circuits in high-performance computing and telecommunications has been rising steadily. In various data processing and telecommunications devices, more and more complex functions are required. The need to integrate these functions in a small system is also increasing.

Due to the current demand in communication technology, the proposed Fractional-N phase-locked loop or phase lock loop (PLL) is decided to design using 45 nanometre (nm) CMOS/VLSI technology to achieve the low power consumption and high stability. The main novelties related to the 45nm technology are the high-k gate oxide, metal gate and very low-k interconnect dielectric. The effective gate length required for 45 nm technology is 25nm. Here for the design using VLSI technology, micro wind 3.1VLSI backend software is used. This software allows designing and simulating an integrated circuit at physical description level. For low power, low leakage transistors will be used and will Compromise on little bit frequency.

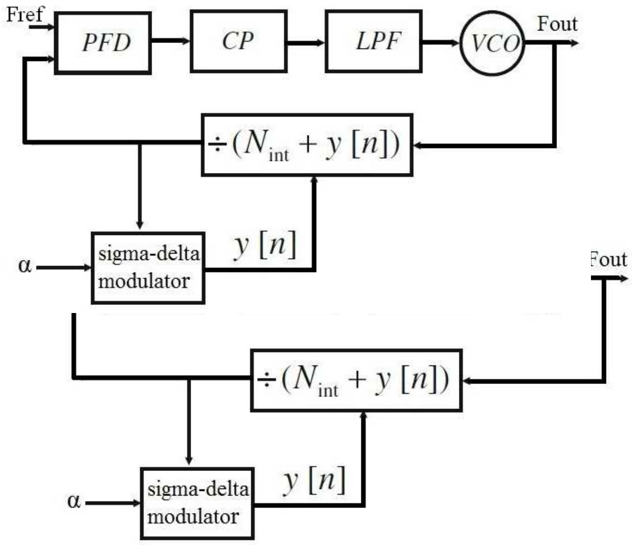


**Figure 2. Block Diagram of PLL using Sigma-delta fractional –N frequency synthesizer**

The proposed fractional N-PLL is shown in figure 2. It consist of Phase detector, low pass filter, charge pump, voltage controlled oscillator and Sigma delta modulator. Phase detector is a comparator that compares the input frequency fs with output frequency of VCO and generates a d.c voltage that is proportional to the phase difference between the two frequencies. The function of the low pass filter is to remove high frequency components from the output of the phase detector. This low pass filter controls other characteristics of the PLL including bandwidth, capture range, lock range and transient response.The VCO is the most important functional unit in the PLL. The VCO is commonly used for clock generation in phase lock loop circuits. Its output frequency determines the effectiveness of PLL.

The proposed work consists of additional sigma delta modulator block with fractional input. This block gives DC output proportional to the fractional inputs which then add with divide by N integer value.

**LITERATURE REVIEW**

Many researchers design the PLL by applying many Mathematical & Logical expressions by using different phenomenon or processes for finding various parameters.

One of the important implementation of phase lock loop is the fractional-N frequency synthesizer using Sigma-Delta modulation technique which offers a short switching time and a good noise reduction performance. A loop filter offers the best suppression to the quantization noise at high frequencies. The simulation results showed that chosen bandwidth and phase margin yield fast switching time and the modulator had very good suppression to the fractional spurs[1].

Another important PLL is designed and analyzed using 45nmCMOS/VLSI with micro wind 3.1 with four multiple outputs which provides high efficient, optimum area chip with low power in milliwatt and four multiple outputs with high stability[2].

The another design of PLL, includes the design of charge pump for low voltage devices. CMOS charge pump circuit uses both the NMOS switches and the PMOS switches. The simulation result showed that higher pumping efficiency can be achieved by the proposed charge pump compared with the others[3].

**IMPLIMENTATION OF PLL USING 45 nm VLSI TECHNOLOGY**

**Phase detector**

The first block of Phase Locked Loop is the phase detector. The phase detector of the PLL is the XOR gate. The XOR gate output produces a regular square oscillation when the clock input and signal input have one quarter of period shift ($90^0$ or ∏/2). For other angles, the output is no more regular.

Figure 4. shows layout of Phase detector and figure5. shows output waveform.

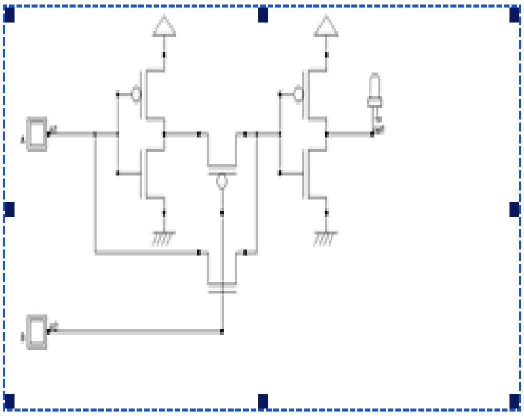

**Figure 3.CMOS circuit of Phase Detector**

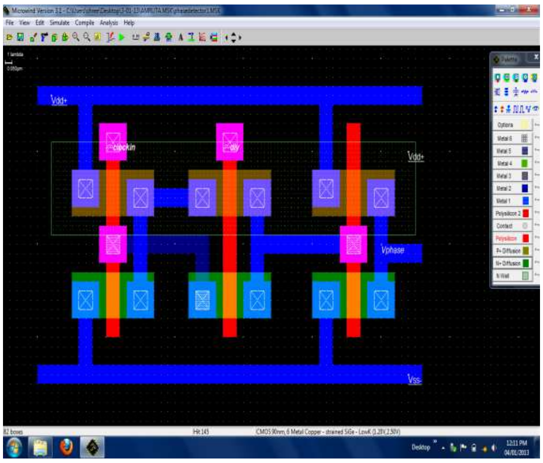

**Figure 4.Layout of Phase Detector**

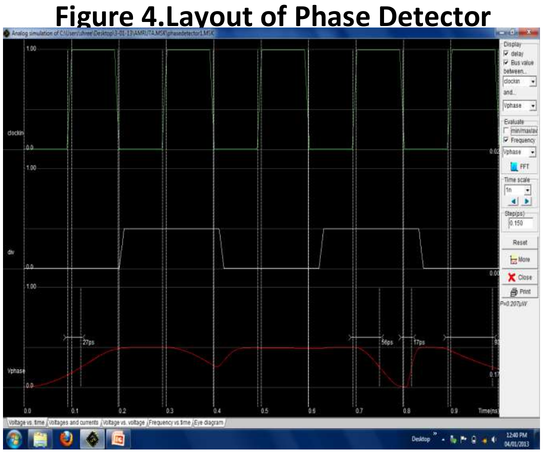

**Figure 5.Voltage vs Time output**

**Loop filter**

The filter may simply be a large capacitor C charged and discharged through the $R_{on}$ resistance of the switch. The $R_{on}.C$ delay creates a low-pass filter. Figure 6. Shows a CMOS circuit of XOR gate with the output charged with a large capacitor and a serial resistance to create the desired analog control voltage.

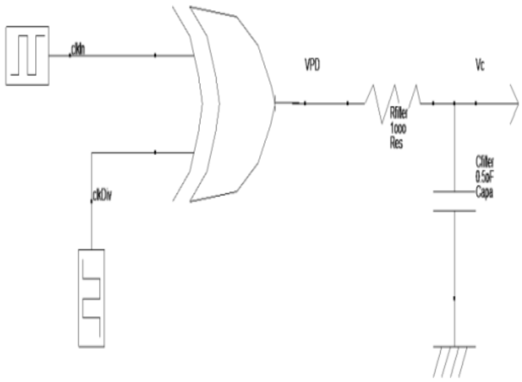

**Figure 6.CMOS circuit of Filter**

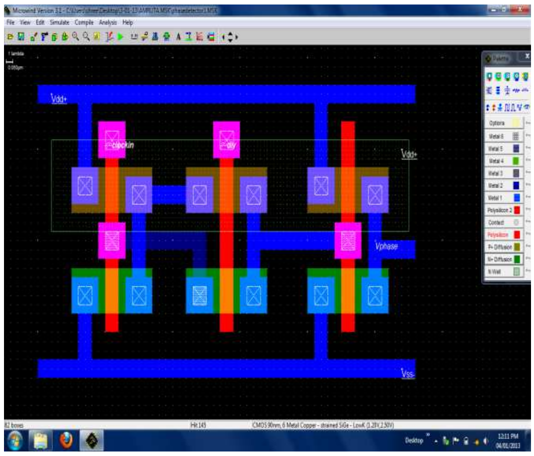

**Figure 7.Layout of Loop filter**

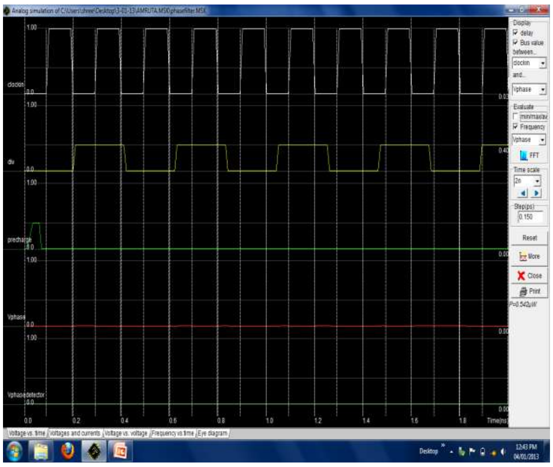

**Figure 8.Voltage vs Time output**

**CONCLUSION**

To implement fractional N-PLL using VLSI technology, first each block of PLL such as Phase detector, loop filter had been implemented using 45nm CMOS technology with microwind 3.1 backend software of VLSI. For individual blocks of PLL, analog circuits are designed using CMOS transistor and power consumption found less. Thus very efficiently phase detector and loop filter are designed. In remaining part of design all these blocks will be cascaded to have the fractional N-PLL.

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Using The PLL Design Assistant and CppSim

Programs”