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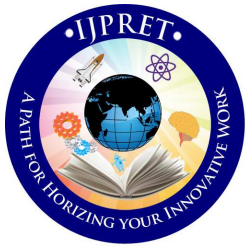

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A PATH FOR HORIZING YOUR INNOVATIVE WORK

VLSI IMPLEMENTATION OF NEURAL NETWORK

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Abstract

Artificial intelligence is realized based on mathematical equations and artificial neurons. In the proposed design our main focus is on the implementation of Neural Network Architecture (NNA) on a chip in VLSI for generic signal processing applications. The analog components like Gilbert Cell Multiplier (GCM), Adders, Neuron activation Function (NAF) will be used in the implementation. This neural architecture is trained using Back propagation (BP) algorithm in analog domain with new techniques of weight storage. We are using 45nm CMOS technology for layout designing and verification of proposed neural network. The functionality of proposed design of neural network will be verified for analog operations like signal amplification and frequency multiplication.

INTRODUCTION

Intelligence is the computational part of the ability to achieve goals in the world. This intelligence though a biological word, is realized based on the mathematical equations, giving rise to the science of Artificial Intelligence(AI). To implement this intelligence artificial neurons are used.

These artificial neurons comprised of several analog components. The neuron selected is comprises of multiplier and adder along with the tan-sigmoid function. The training algorithm used is performed in analog domain thus the whole neural architecture is analog structure. The proposed technology is a step in the implementation of neural network architecture using back propagation algorithm. These artificial neurons, we are realizing by Analog components like multipliers, adders and differentiators.

The proposed work is aimed to achieve the low power consumption, high stability of output. The electronics industry has achieved a phenomenal growth over the last two decades, mainly due to the rapid advances in integration technologies, large-scale systems design - in short, due to the advent of VLSI Technology. The number of applications of integrated circuits in high-performance computing telecommunications, and consumer electronics has been rising steadily, and at a very fast pace. Typically, the required computational power (or, in other words, the intelligence) of these applications is the driving force for the fast development of this field.

Certain advantages of VLSI technology are:

- Less area/volume and therefore, compactness
- Less power consumption
- Less testing requirements at system level
- Higher reliability, mainly due to improved on-chip interconnects
- Higher speed, due to significantly reduced interconnection length
- Significant cost savings

LITERATURE REVIEW

From the rigorous review of related work and published literature, it is observed that many researchers have designed Artificial Neural Network by applying different techniques. Since in the real world today VLSI/CMOS is in very much in demand,

fromthe careful study of reported work it is observed that few researchers have taken a work for designing Artificial Neural Network with CMOS/VLSI technology.

- Yammenavar in year 2011 proposed Design And Analog VLSI Implementation Of Artificial Neural Network which was having one layer of neural network using 180nm CMOS technology.[Yammenavar et.al, 2011]
- NeerajChasta in the year 2012 proposed Analog VLSI Implementation of Neural Network Architecture with two layers for Signal Processing using 500nm CMOS technology. [NeerajChasta et.al, 2012]

As an improvement in above designed parameters the proposed design is aimed to have two layered feed forward neural network in which we are using 45nm CMOS technology.

PROPOSED WORK

The technology we are using to convert the given network in analog VLSI chip is 45nm CMOS technology. The main novelties related to the 45 nm technology are the high-k gate oxide, metal gate and very low-k interconnect dielectric. The effective gate length required for 45 nm technology is 25nm.

Compared to 90-nm and 65 -nm technology, 45 nm technologies must offer:

- 30% increases in switching performance
- 30 % reduction in Power consumption
- 2 times higher density
- 2 times reduction of the leakage between source and drain and through the gate oxide.

Considering the advantage of 45 nm technologies over 90 nm & 65 nm technologies, the proposed work is done with 45 nm technology.

The analog components used are comprises of multipliers and adders along with the tan-sigmoid function circuit.

The proposed neural architecture will be capable of performing operations like sine wave learning, amplification and frequency multiplication and can also be used for analog signal processing activities

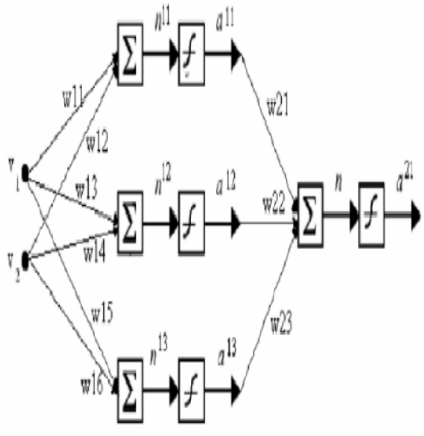

Figure : Layered structure of Neural Network

Figure: 1

The neural network is shown in the above figure. In this network, inputs are applied with the weight matrix, then this weighted inputs of the adder are summed up. The output generated by adder blocks is given to the Neuron Activation function. The output of activation function is multiplied by weights again and given to the input blocks of output layer.

This layered structure of neural network is implemented in VLSI using analog components. Gilbert cell multiplier, adder and differential amplifiers are used for different blocks.

DESIGNED PART

Neuron:

Neurons use sigmoidal type activation functions. sigmoidal type functions allow simple networks the ability to describe complex surfaces.

Nonlinear activation functions of neurons are essential for neural network operation. Such sigmoidal functions can be created in the differential pair.

The schematic, VLSI layout and simulation of sigmoidal function is as shown below.

Schematic of sigmoidal function

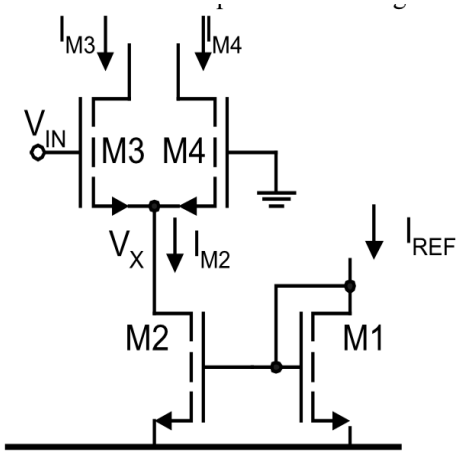

Figure: 2Layout of sigmoidal function

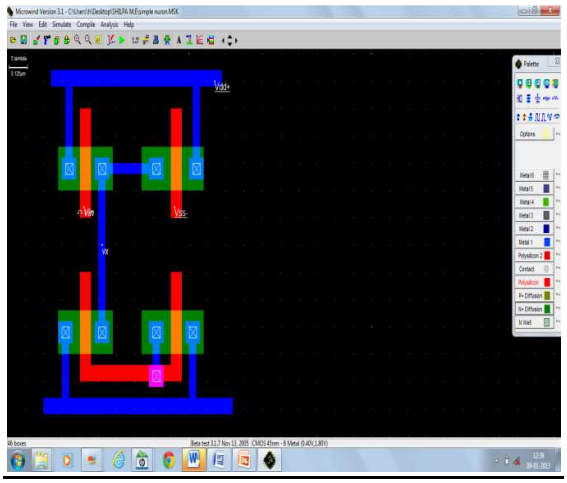

Figure: 3Simulation of sigmoidal function

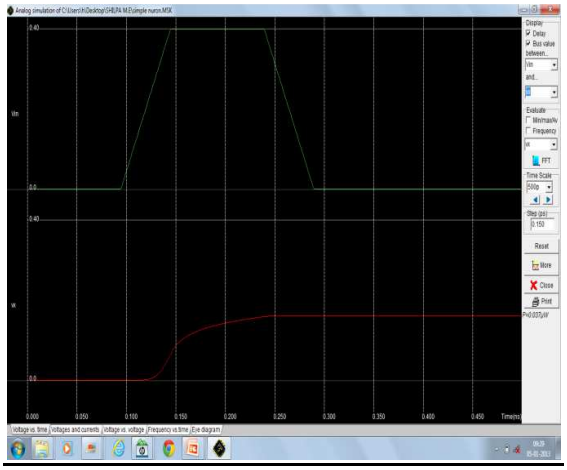

Figure: 4

Gilbert cell:

The Gilbert cell is used as the multiplier block. The main building blocks of Gilbert cell are differential pair transistors, current mirror circuit.

The schematic diagram, layout structure and simulation of the Gilbert cell is as shown below.

Schematic of gilbert cell

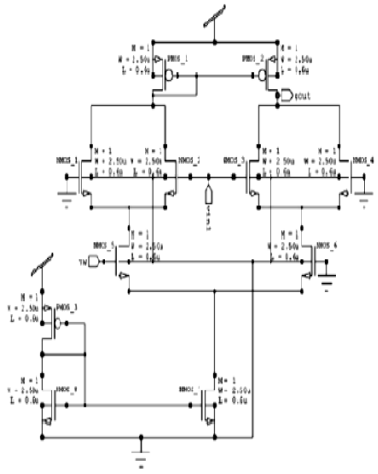

Figure: 5Layout of gilbert cell

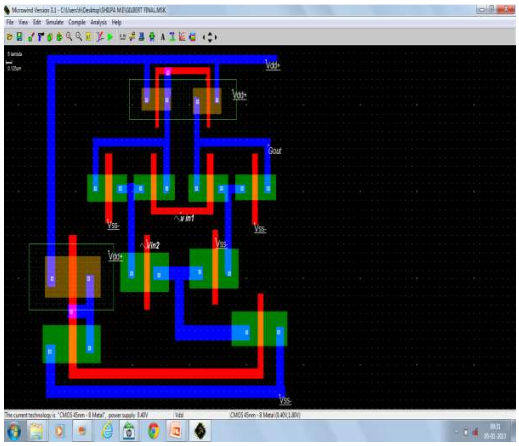

Figure: 6Simulation of gilbert cell

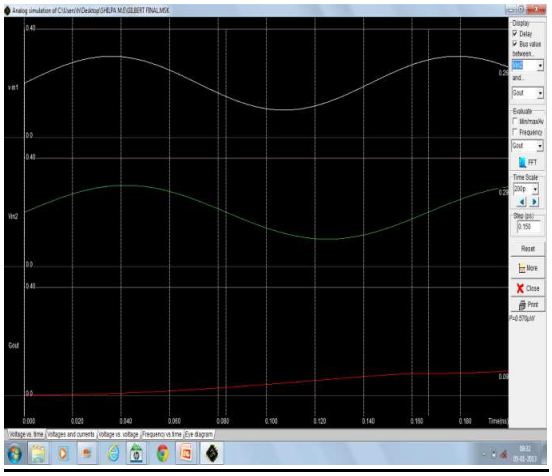

Figure: 7

CONCLUSION

To implement feed forward neural network using VLSI technology, first each block of neural network such as neuron activation function, Gilbert cell had been implemented using 45nm CMOS technology with backend software of VLSI micro wind 3.1. Results obtained are as per the expectations. In the remaining part of design all these blocks will be cascaded to have feed forward neural network. For individual blocks of network i.e. neuron activation function, Gilbert cell analog circuits are designed using CMOS transistors and power consumption is found to be very less. Thus very efficiently neuron activation function, Gilbert cell are designed.

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