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ANALYSIS AND IMPLEMENTATION OF MAC WITH WALLACE TREE

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Abstract

Designing of MAC having high speed & low power is research of interest. Real-time signal processing requires high speed and high throughput Multiplier-Accumulator (MAC) unit that consumes low power, which is always a key to achieve a high performance digital signal processing system. This paper proposes work of design and implementation of a low power MAC unit. Firstly, a MAC unit is designed, with appropriate geometries that gives optimised power, area.8*8 bit modified Wallace tree construction have been used in this MAC as multiplier which is high speed , low power. Wallace high-speed multiplier uses full adders and half adders, 4:2 compressor, 3:2 compressor in their reduction phase.

INTRODUCTION

In the majority of digital signal processing (DSP) applications the critical operations usually involve many multiplications and/or accumulations. For real-time signal processing, a high speed and high throughput Multiplier-Accumulator (MAC) is always a key to achieve a high performance digital signal processing system. In the last few years, the main consideration of MAC design is to enhance its speed. This is because; speed and throughput rate is always the concern of digital signal processing system. But for the epoch of personal communication, low power design also becomes another main design consideration. This is because; battery energy available for these portable products limits the power consumption of the system. Therefore, the main motivation of this work is to investigate various pipelined multiplier/accumulator architectures and circuit design techniques which are suitable for implementing high throughput signal processing algorithms and at the same time achieve low power consumption. A conventional MAC unit consists of (fast multiplier) multiplier and an accumulator that contains the sum of the previous consecutive products. The function of the MAC unit is given by the following equation: F = Σ A i Bi

Figure 1: Basic structure of MAC

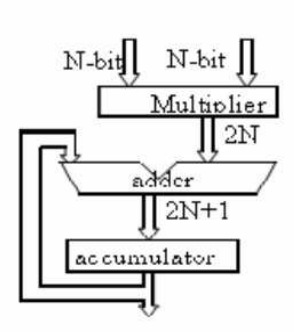
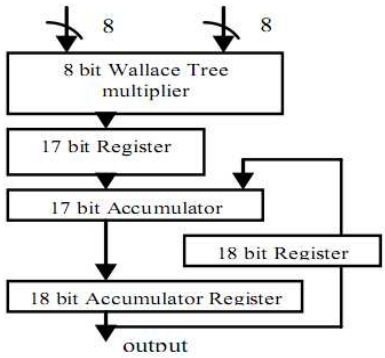


Figure 2: MAC architecture



Original MAC

The main goal of a DSP processor design is to enhance the speed of the MAC unit, and at the same time limit the power consumption. In a pipelined MAC circuit, the delay of pipeline stage is the delay of a 1-bit full adder. Estimating this delay will assist in identifying the overall delay of the

pipelined MAC. In this work, full adder is designed. Area, power is calculated for the full adder, based on which the pipelined MAC unit is designed for low power.

CONSTRUCTION OF MAC

In this paper the MAC can be constructed by using latches, Wallace tree multiplier & adder. Wallace tree multiplier uses half adder, full adder, 4:2 compressor & 3:2 compressor in their reduction phase.

OPTIMIZATION

The circuits produced by contemporary VHDL synthesis tools are, unfortunately, highly sensitive to the manner in which the original behavioral or structural description is expressed. While designing the MAC having Wallacetree multiplier, using different VHDL constructs to describe the same behavior resulted in a faster and smaller design. When describing circuits in VHDL, carefully some aspects should be taken into account. The synthesis tools sensitive to behavioral or structural descriptions.

IMPLEMENTATION IN VHDL

VHDL can be used to represent several levels of abstraction. The level chosen to represent MAC includes a mixture of register- level and gate –level logic blocks. To describe the register transfer level and the data flow through the multiplier, VHDL constructs Called processes provide the sequential instructions that manipulate data. Each process contains a sensitivity list that triggers the actions within a process.

VERIFICATION OFSIMULATION

Quartus II is powerful simulation tool developed by Altera Technologies for altera devices. VHDL code can be compiled and special libraries for altera devices can be used to simulate any hardware efficiently. All the basic modules designed for MAC are compiled and tested vigorously for functional correctness using waveforms. The complete circuit of MAC including 8*8 bit Wallace tree multiplier is described in VHDL, as a structural component. The hierartial structure is created and the complete simulation can be observed. Fig.3 shows the waveform simulation result for the MAC including Wallace tree multiplier.

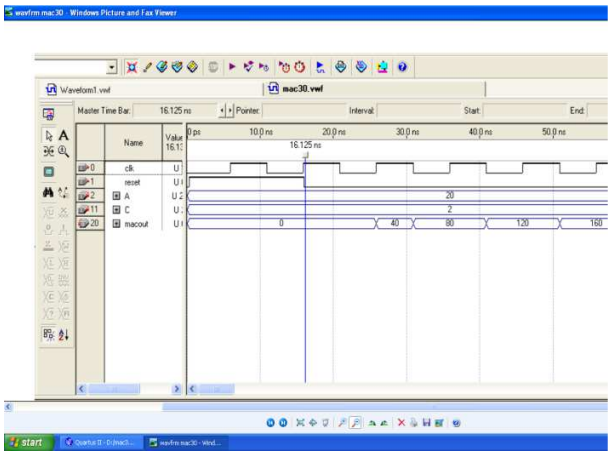
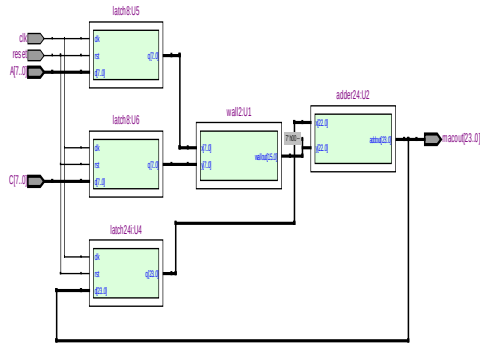


Fig 3. Simulation waveform of MAC

RTL VIEW



POWER & AREA ANALYSIS

Powerplay Power Analyzer status: Successful – Wed Feb13 22:42:28 2013

Quartus II Version : 8.1 Build 163 10/28/2008 SJ Web Edition

Revision Name: mac30

Top-level Entity Name: mac30

Family: Cyclone II

Device: EP2C20F484C

Power Models: Final

Total Thermal Power Dissipation: 124.59 mW

Power Core Dynamic Thermal Dissipation: 7.08mW

Power Core Static Thermal Dissipation: 47.45mW

I/O Thermal Power Dissipation : 70.06 mW

Total Logic Elements : 179 / 18,752(<1%)

Total Combinational Function: 179 / 18,752(< 1%)

Dedicated Logic register: 39/ 18,752(< 0%)

Total Registers : 39

Total Pins : 42 / 315 (< 13%)

Total Virtual Pins : 0

Total Memory Bits : 0 / 239,616 (< 0%)

Embedded Multiplier 9-bit Elements : 0 / 52 (0 %)

CONCLUSION

The MAC can be solved & analyzed using a new modified method of Wallace tree construction. The modified tree has a slightly smaller critical path ,a slightly larger wiring overhead but requires low power and high speed. A 8x8 bits Wallace tree multiplier was designed in 0.25µm.As per analysis the power core dynamic thermal dissipation is 7.08mW which is much less.

Total logic elements and total combinational functions required are only less than1% from the available. There is no requirement of logic registers, registers, pins memory bits and PLLs.

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