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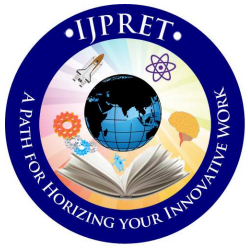

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REVIEW ON AREA AND POWER EFFICIENT ROUTER FOR NETWORK ON CHIP TECHNOLOGY

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Abstract

As chip manufacturing technology shrinks toward sub-nanometers, a chip die will comprise more and more of processing blocks. Interconnection, communication, and utilization of shared resources of these blocks are getting more complicated for System-on-Chip (SoC). Network-on-chip (NoC), one of the most promising interconnection schemes for complex SoC design, presents large design space. Because the influence of different parameters on the performance of the NoC varies significantly, it is desirable to analyze and understand specific effect of these parameters on the overall performance in order to provide NoC designers guidelines to optimize their plans. This paper gives the review of different on-chip routers based on optimizing power consumption and chip area. Proposed architecture of on-chip router in this paper may give the results in which power consumption is reduced and silicon area should also minimize.

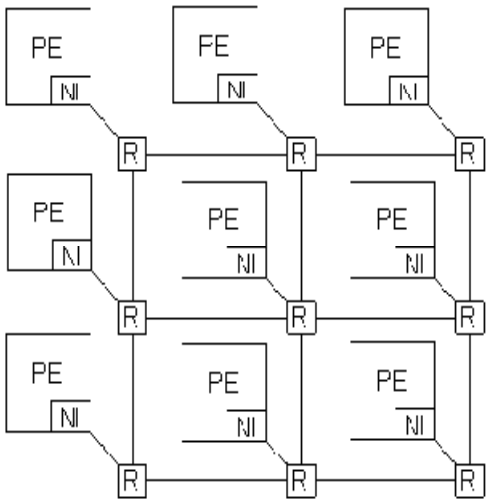
1. INTRODUCTION

The Network-on-Chip (NoC) paradigm has evolved to replace ad-hoc global wiring interconnects. With this approach, system modules communicate by sending packets to one another over a network. In Modern VLSI Systems Power consumption is becoming a crucial.

l factor in the design of high-speed digital systems. The structured NoC wiring allows for the use of high-performance circuits to reduce latency and increase bandwidth. The on chip router's micro architecture plays a vital role in achieving these performance goals.

1.1Network on chip

There are different interconnection schemes are currently in use which includes buses, crossbar, and NOCs. Out of these above schemes buses and NOCs are dominant in research community. However buses suffer from poor scalability because as the number of processing elements increases, performance degrades dramatically. Hence they are not considered where processing elements are more. To overcome this limitation attention has shifted to packet-based on-chip communication networks, known as Network-On-Chip (NOC).



PE – Processing Element

R – Router

NI – Network Interface

Fig: 1. NOC Architecture

A typical NoC consists of computational processing elements (PEs), network interfaces (NIs), and routers. The NI is used to packetize data before using the router backbone to traverse the NoC. Each PE is attached to an NI which connects the PE to a local router. When a packet was sent from a source PE to a destination PE, the packet is forwarded hop by hop on the network via

the decision made by each router. For each router, the packet is first received and stored at an input buffer. Then the control logics in the router are responsible to make routing decision and channel arbitration. Finally, the granted packet will traverse through a crossbar to the next router, and until the packet arrives at its destination the process repeated.

1.2 On-Chip Router

The router is the heart of an on-chip network, which undertakes crucial task of coordinating the data flow. The router operation revolves around two fundamental regimes: (a) the data path and (b) the associated control logic. The data path consists of number of input and output channels to facilitated packet switching and traversal. Generally 5 input X 5 output router is used. Out of five ports four ports are in cardinal direction (North, South, East, and Waste) and one port is attached to its local processing element.

Like in any other network, router is the most important component for the design of communication back-bone of a NoCsystem. In a packet switched network, the functionality of the router is to forward an incoming packet to the destination resource if it is directly connected to it, or to forward the packet to another router connected to it. It is very important that design of a NoC router should be as simple as possible because as the complexity of router increases, implementation cost also increases.

2. LITERATURE REVIEW

In this section, we summarize prior research onNoC architectures and other work related to our design.

In 2009 V.Soteriou, R.S. Ramanujam, B. Lin and Li-ShiuanPehl [1] proposed the router for NOC to increase throughput of the network and they introduces architecture which shows a significant improvement in throughput at the expense of area and power due to extra crossbar and complex arbitration scheme. They get upto 94% of throughput but power consumption is increased by the factor of 1.28. Our approach may give the reduced power consumption.

In 2009 A. Kodi, A. Louri, J. Wang [2] illustrates the impact of repeater insertion on inter-router links with adaptive control and eliminating some of the buffers in the

router. Their approach saves appreciable amount of power and area without significant degradation in the throughput and latency. But there is still some scope to increase the buffer utilization inside the router.

In 2011 Ying-CherngLan, Shih-Hsin Lo, Yueh-Chi Lin and Yu-Hen Hu et. al [3] addresses the buffer utilization by making the channels bidirectional and shows significant improvement in system performance. But in this case, each channel controller will have two additional tasks: dynamically configuring the channel direction and to allocate the channel to one of the routers, sharing the channel. Also, there is a 40% area overhead over the typical NoC router architecture due to double crossbar design and control logic.

In 2009 M. H. Neishaburi,ZeljkoZilic [4] proposed the router architecture with Reliability Aware Virtual Router. In this architecture they allocate more memory to the busy channels and less to the idle channels. This dynamic allocation of storage shows 7.1% and 3.1% latency decrease under uniform and transposes traffic patterns respectively at the expense of complex memory control logic. Though this solution is latency efficient but not area and power efficient

In 2006 M. Coenen [5] proposed an algorithm to optimize size of decoupling buffers in network interfaces. The buffer size is proportional to the maximum difference between the number of words produced and the number of words consumed at any point in time. This approach showed significant improvement in power dissipation and silicon area. The buffer size can be further optimized by considering the idle time of buffer. If some buffer is idle at some time instant, it can share the load of neighboring input channel and thus increase the utilization of existing resources with small control logic.

3. PROPOSED ROUTER ARCHITECTURE

The router architecture can be divided into two parts, the Input and the output. The Input part is responsible for buffer allocation and receiving the packets from neighboring routers. The Output part computes the route and transmits the packets accordingly. Within the router, the Input and the Output parts do not

communicate at all. Both parts simply write and read from the buffers.

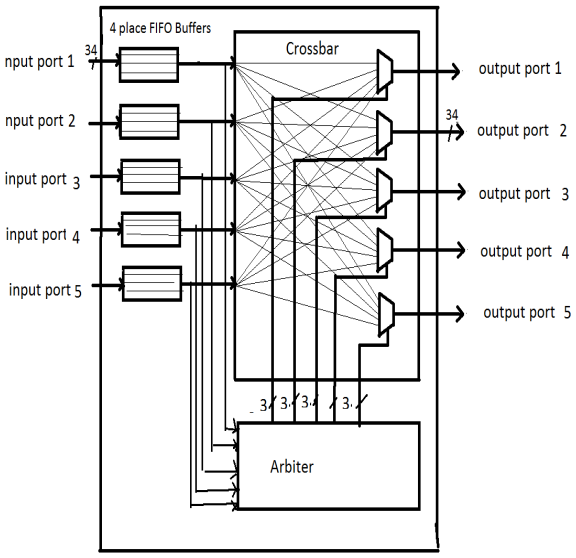


Fig: 2. 5 Input 5 Output port On-Chip Router

The proposed architecture consists of mainly three parts:

1. FIFO Buffer
2. Crossbar Switch
3. Arbiter

FiFo (First in First out) Buffer is used in NoC Router for storage of packet of input port. Matrix Arbiter is used to trap the source and destination address of input and output port. Matrix Arbiter generates the control signal according to priority so that Crossbar switch transmits data from source to destination.

1. FIFO Buffer :

FIFO Buffer is used as input buffer to store the data temporarily. FSM controls the read and write operation of FIFO according to its status. If FIFO Buffer is empty and having space to store the data, FSM will generate acknowledgement signal in respect to the request coming to input channel, thus write operation starts. If FIFO Buffer is full or not having space to store the data, the write operation stops and the acknowledgement signal goes low. When the FIFO Buffer is full, FSM will send request to output channel of other port, if grant signal is received by it then read operation starts and continues until grant signal goes low or FIFO Buffer empties. Thus empty status of indicates the end of communication.

2. Crossbar Switch:

A crossbar switch (also known as cross-point switch or matrix switch) is a switch connecting multiple inputs to multiple outputs in a matrix manner. In the

proposed architecture of router 5 input 5 output type of crossbar switch is used.

Five 5:1 multiplexers are used, one at each input to the crossbar. All the inputs to the crossbar is fed to each multiplexer. Which input is forwarded to the output is decided by the select lines generated by the arbiter. This feature avoids the Head of Blocking Problem which is usually occurs in conventional crossbar switches.

3. Arbiter:

Depending on the control logic arbiter sets the select lines of the multiplexers inside the crossbar switch. The overall functioning of crossbar is totally depending on the arbiter control logic.

The arbiter traps the source and destination address from the output 0f buffer and generate the control signal so that input data from source side sending to the output port. It also controls the arbitration of the ports and resolves contention problem. It keeps the updated status of all the ports and knows which ports are free and which ports are communicating with each other.

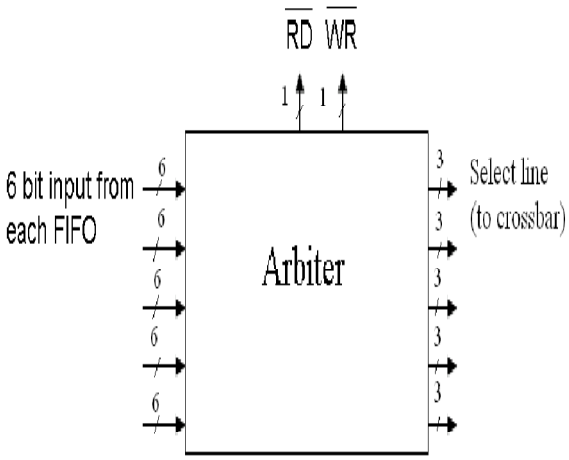


Fig: 3. Arbiter

The proposed router architecture uses Round Robin Arbitration Algorithm. It operates on the principle that the request that was just served should have the lowest priority on the next round of arbitration. It is desirable that the arbitration algorithm used must be efficient.

Round Robin Arbitration

Packets with the same priority and destined for the same output port are scheduled with a round-robin arbiter. Supposing in a given period of time, there was many input ports request the same output or resource, the arbiter is in charge of processing the priorities among many different request inputs. The arbiter will release the output port which is connected to the crossbar once the last packet has finished transmission. So that other waiting packets

could use the output by the arbitration of arbiter. A round-robin arbiter operates on the principle that a request which was just served should have the lowest priority on the next round of arbitration. Depending upon the control logic arbiter generates select lines for multiplexer based crossbar and read or write signal for FIFO buffers.

4. CONCLUSION

In the current silicon era, NoC is not power and area efficient although it has higher throughput. The proposed architecture will show significant reduction in silicon area and power consumption. As the buffers can be shared by a couple of input ports in our architecture, significant improvement in buffer utilization will also be achieved with limited resources.

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