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IMPROVED PERFORMANCE OF SPLIT CAPACITOR BASED DSTATCOM FOR SHUNT APPLICATION

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Abstract

This paper presents inverter topologies for low voltage Distribution system. Hysteresis current control scheme has been suggested. These inverters is operated in current control mode by suitable control strategy, to compensate DC component in load neutral current, load compensation, power factor correction. The reference currents are generated by instantaneous symmetrical current component theory. Simulations are done by MATLAB.

INTRODUCTION

The different power quality problems like voltage sag , swell , unbalanced , voltage waveform distortion [2-5]and the implementation of custom power devices for the mitigation of various PQ issues are suggested [5-6]. It was also proposed their exist different inverter topologies for low and high voltage distribution system [1] with the different control strategies generally used for inverters [6]. The switching strategy for the inverter topologies and generating the reference current from the instantaneous symmetrical component theory was suggested [6,7]

Power quality is the important issue now a day's. Power Quality (PQ) related issues are of most concern nowadays, the main cause of power quality problems are power electronic equipment, information technology equipments, adjustable speed drives (ASD),& etc; because of which load cause disturbance in voltage waveform. There can be different power quality problems arises generally in distribution systems, like voltage sag, swell, unbalanced, waveform distortion etc. There are certain power quality issues related to current also, like unity power factor, voltage regulation (combinely known as load compensation), harmonic current compensation, neutral current compensation etc. Hence the main aim of load compensation is to get unity power factor and minimum voltage regulation.

To mitigate the above mentioned power quality problems various generalized methods have been suggested in the literature. One of the important methods is by using custom power devices like Distribution static compensator (DSTATCOM), Dynamic voltage restorer and Unified power quality conditioner (UPQC). Among all the DSTATCOM is a powerful custom power device having multiple applications like voltage regulation, unity power factor and harmonic current compensation. It is also used to mitigate the voltage related issues.

In this project different Inverter topologies are used to implement DSTATCOM for low and high voltage distribution system.

DSTATCOM is shunt connected device at load side injects appropriate controlled

current into the line. It basically comprises of Voltage Source Inverter (VSI) structure because it can be extended to multilevel, multi-chain and multi-cells structure. For low voltage distribution system three different inverter topologies are used like three leg VSC with single DC capacitor, three leg VSC with neutral clamped DC capacitor and Three phase four leg VSC.

For high voltage distribution system different inverter topologies are four legs VSC with single DC capacitor, three leg VSC with neutral clamped DC capacitors and three independent single phase inverter with single dc capacitor.

For modulation different pulse width modulation (PWM) are used. In this project all the above topologies will be realized using hysteresis current controlled pulse width modulation

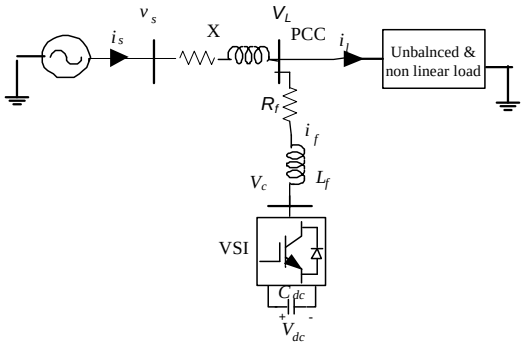
and for the generating the reference current ,the instantaneous symmetrical component theory will be used.

Different inverter topologies for low voltage distribution system

a) Three phase three leg inverter with single dc capacitor.

b) Three phase three leg inverter with split dc capacitor.

Basic single line diagram of DSTATCOM



Fig(1) DSTATCOM structure.

Above fig (1) shows the single line diagram of DSTATCOM. It consist of three components Inverter, interface inductor and DC link. Hysteresis current control modulation is used for switching of DSTATCOM. It is a shunt compensated device injects the compensated current at the point of common coupling (PCC).

Reference current generation

Different methods of reference current generation like Instantaneous PQ theory,

Synchronous detection technique and Instantaneous symmetrical component theory. Instantaneous symmetrical component theory is the simplest theory to implement.

The reference currents are generated by the equations given in (1).

$$\left.\begin{aligned} i_{far} &= i_{la} - \frac{v_{sa} + (v_{sb} - v_{sc})\beta}{v_{sa}^2 + v_{sb}^2 + v_{sc}^2}(plav) \\ i_{fbr} &= i_{lb} - \frac{v_{sb} + (v_{sb} - v_{sa})\beta}{v_{sa}^2 + v_{sb}^2 + v_{sc}^2}(plav) \\ i_{fcr} &= i_{lc} - \frac{v_{sc} + (v_{sa} - v_{sb})\beta}{v_{sa}^2 + v_{sb}^2 + v_{sc}^2}(plav) \end{aligned}\right\} \quad (1)$$

If we consider inverter losses then the equations are given in (2).

$$\left.\begin{aligned} i_{far} &= i_{la} - \frac{v_{sa} + (v_{sb} - v_{sc})\beta}{v_{sa}^2 + v_{sb}^2 + v_{sc}^2}(plav + ploss) \\ i_{fbr} &= i_{lb} - \frac{v_{sb} + (v_{sb} - v_{sa})\beta}{v_{sa}^2 + v_{sb}^2 + v_{sc}^2}(plav + ploss) \\ i_{fcr} &= i_{lc} - \frac{v_{sc} + (v_{sa} - v_{sb})\beta}{v_{sa}^2 + v_{sb}^2 + v_{sc}^2}(plav + ploss) \end{aligned}\right\} \quad (2)$$

Low Voltage distribution system

In a VSC structure, each switch contains an Insulated Gate Bipolar Transistor (IGBT) with its associated anti-parallel diode. All the VSC topologies discussed below for low voltage distribution systems. It is connected to three phase four wire(3p4w) system through interface inductor.

Three leg VSC with single dc capacitor

Fig. 2 shows the schematic diagram of three leg VSC with single dc capacitor. It consists of six switches. The operation depends on the control strategy used. Hysteresis current control has been used for the control the switching of the VSC. It connected to 3p4w system through interface inductor. The reference current having zero sequence component but in this topology not having path to inject zero sequence component to compensate the neutral current.

Simulation results are as shown in fig (3) (a)-(d). For the balanced load with balanced source there is no need to compensation. Simulation results for unbalanced load as shown in fig (4)(a)-(f). Because of unbalanced load causes zero sequence current presents in the system at load side it cause unbalanced to source voltage as well as source current. But this

topology is unable to compensate source current. Fig. 4(a) and (b) shows tracking of reference current and injected currents for only few portion of cycle fails to track phase '*a*' and '*b*'. Only phase '*c*' current tracks exactly as shown in Fig. 4 (c). The loss of tracking is because the zero sequence components are present in reference while VSI is not able to inject the current having zero sequence components. This topology is not compensates the source current as well as not neutralize the neutral current. The full compensation will not be possible as the zero sequence components in the load current. Modify the reference currents given by equations (7) & (8). Modified the reference currents by eliminate the zero sequence component from load current. The improved results are as shown in Fig 5 (a)-(f).

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System parameters

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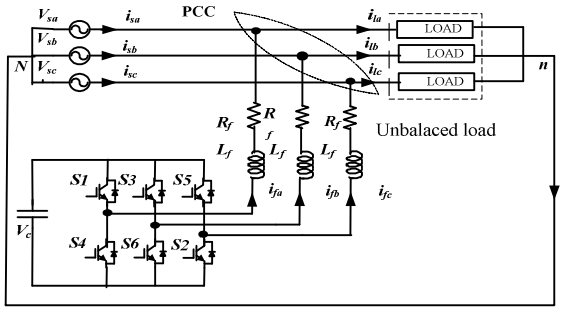


Fig (2) Three leg VSC with single DC capacitor.

Simulation result of three leg VSC with single dc capacitor for balanced load

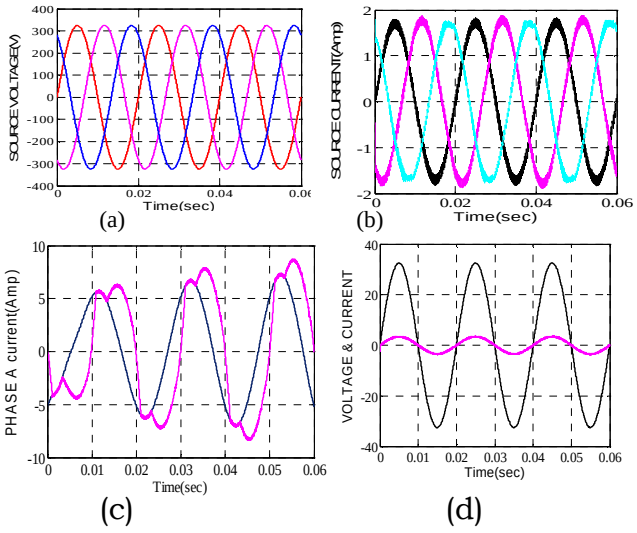


Fig (3) Simulation of three-leg VSC with balanced load: (a) source voltage; (b) Source currents; (c) load currents; (d) source voltage and current.

Simulation results for Three phase single dc capacitor with unbalanced load

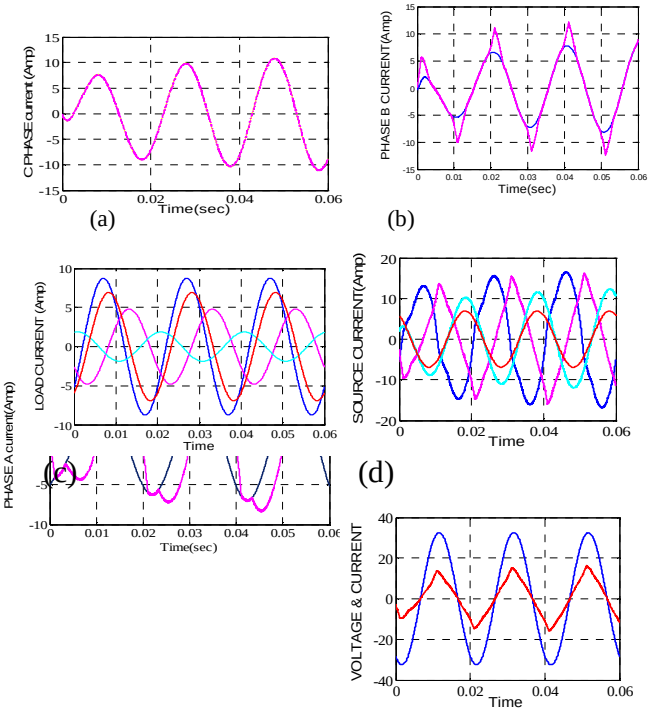


Fig.(4) Simulation of three-leg VSC for unbalanced load:(a) phase a injected Currents (b) phase b injected currents; (c) phase c injected currents; (d) compensated source currents; (e) load currents; (f) source voltage and current

$$i_{lo} = \frac{I_{la} + I_{lb} + I_{lc}}{\sqrt{3}}$$

(3)

For the modified reference current the equation is follows

$$I'_{\beta kr} = I_{\beta Kr} - \frac{i_{lo}}{\sqrt{3}}$$

(4)

Simulation results for unbalanced load with modified reference

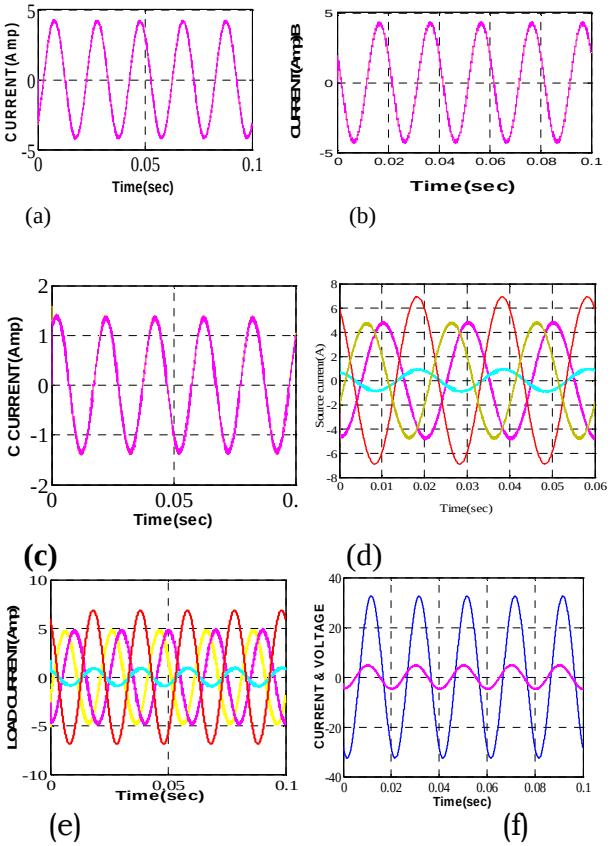
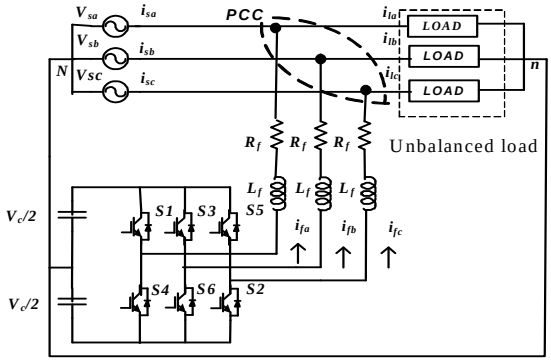


Fig.(5) Simulation of three-leg VSC for unbalanced load with modified reference currents: (a) phase a injected currents; (b) phase b injected currents; (c) phase c injected currents; (d) compensated source currents; (e) load currents; (f) source voltage and current.

Improved simulation results are as shown in Fig (5) (a)-(c) with modified reference currents but still not compensate the neutral current.

Three leg VSC with neutral clamped dc capacitor

Fig (6) shows the three leg VSC with neutral clamped dc capacitor diagram. Zero sequence current component compensate by injecting the compensated current into the line.

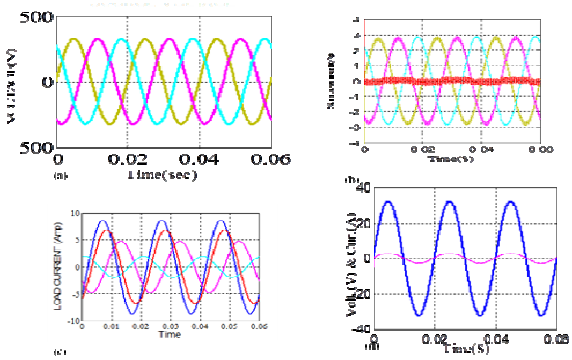


Fig(6) Three phase three leg with split dc capacitor.

In this topology, neutral point of inverter (N') connected to neutral of source (N) and neutral of load (n), which is the path to inject zero sequence current to neutralized the zero sequence component at source side.

The zero sequence components present in only when the unbalanced or non linear loads are connected to the 3p4w system. This topology is able to compensate the zero sequence current components. Simulation results of neutral clamped dc capacitor without dc current as shown in Fig (7) (a)-(d). Simulation results of neutral clamped dc capacitor without dc current as shown in Fig (8) (a)-(d). Connect the dc load to phase C to increase the dc component it result shown in Fig(8) (c). In this topology, there is problem of capacitor balancing to balanced the capacitor different methods are suggested.

simulation results of three phase three leg inverter with split capacitor with unbalanced load: (a) source voltage; (b) source current; (c) load current; (d) Voltage & current of phase a.



CONCLUSION

Three phase three leg with single dc capacitor inverter not able to compensate neutral current as

well as not compensate source current. Three phase three leg with neutral clamped dc capacitor compensate neutral current but having capacitor voltage balancing problem.

Table 1. System Parameters

System parameters	Values of parameters
Source voltages	Balanced sinusoids with $V_{sa}=230\angle 0$
Balanced linear load	$R_l + jX_l = 120 + j125.6\Omega$
Unbalanced linear load	$R_{la} + jX_{la} = 30 + j22\Omega$ $R_{lb} + jX_{lb} = 60 + j31.4\Omega$ $R_{lc} + jX_{lc} = 120 + j125.6\Omega$
Non linear load	$R + jX = 150 + j12.56\Omega$
DSTATCOM When battery used	Vdc = 2 kV, $R_f = 0.01\Omega$,L_f = 40 mH, R_f represents the inverter losses

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