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VHDL IMPLEMENTATION OF DIRECT SEQUENCE SPREAD SPECTRUM CDMA TRANSMITTER AND RECEIVER USING FPGA

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Abstract: The Direct Sequence-Code Division Multiple Access (DS-CDMA) is expected to be the major medium access technology in usage for next generation mobile systems owing to its potential capacity enhancement and the robustness against noise. The CDMA is uniquely featured by its spectrum spreading randomization process employing a Pseudo-Noise (PN) sequence, thus is often called the Spread Spectrum Multiple Access (SSMA). As different CDMA users take different PN sequences each CDMA receiver can discriminate and detect its signal by regarding the signals transmitted by other users as noise-like interferences. In this project Direct sequence principle based CDMA transmitter and receiver will be implemented in VHDL for FPGA based SOC solutions. The digital frequency synthesizer principle is used in generating the carrier signals both at transmitter and receiver modules. The transmitter module mainly consists of programmable PN sequence generator, digital local oscillator, spreader and BPSK modulator blocks. The receiver module consists of BPSK demodulator, matched filter, programmable PN sequence generator and threshold detector blocks. A Gaussian noisy channel will be simulated using Look up table which adds noise to the transmitted signal. The CDMA receiver gets this input and recovers the data using matched filter.

Keywords: SSMA, BPSK, SOC, VHDL, CDMA, LFSR, FDMA, TDMA, DS-CDMA

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1. INTRODUCTION:

In communication systems an attractive approach for economical, spectral efficient and high quality digital cellular and personal communication services is the use of Direct Sequence-Code Division Multiple Access (DS-CDMA) technique[1] due to its improved privacy and security, increased capacity.

VHDL implementation of DS-CDMA transmitter and receiver has been proposed in this thesis. Every mobile handset and every wireless base station operates on the same frequency spectrum .In order to discriminate one conversation from the other, every handset broadcast a unique code sequence is called as pseudo noise code. In this paper pseudo noise code[2] is generated by using two six bit LFSRs. Code signal is called as chip signal. The chips are modulated by the carrier using a digital modulation technique BPSK. The carrier is generated by using the technique discrete digital frequency synthesizer. CDMA base stations must be able to discriminate this different code sequences in order to distinguish one transmission from other. This discrimination is accomplished by means of a matched code filter .A matched code filter is a filter whose frequency spectrum is exactly designed to match the frequency spectrum of the input signal. Here matched code filter generates the pseudo noise code, generated noise code is correlated with the received code and detecting original data.

2. MULTIPLE ACCESS TECHNIQUES

Multiple access schemes are used to allow many simultaneous users to use the same fixed bandwidth radio spectrum. In any radio system, the bandwidth that is allocated to it is always limited. For mobile phone systems the total bandwidth is typically 50 MHz, which is split in half to provide the forward and reverse links of the system. Sharing of the spectrum is required in order to increase the user capacity of any wireless network. FDMA, TDMA and CDMA are the three major methods of sharing the available bandwidth to multiple users in wireless system. Among these multiple access techniques CDMA provides less interfered and more secured type communication which is of more concern [3].

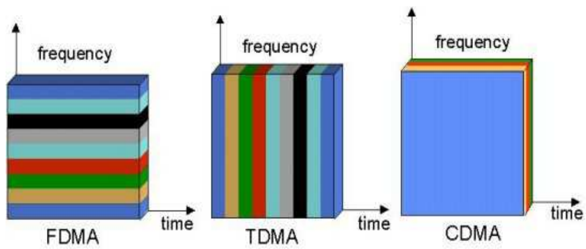

Figure 2.1: Types of Multiple Access Schemes

DIRECT SEQUENCE CDMA GENERATION

DS-CDMA is achieved by spreading the data signal by a pseudo random noise sequence (PN code), which has a chip rate higher than the bit rate of the data. The PN code sequence is a sequence of ones and zeros (called chips), which alternate in a random fashion.

The PN code used to spread the data can be of two main types. A short PN code (typically 10-128 chips in length) can be used to modulate each data bit. The short PN code is then repeated for every data bit allowing for quick and simple synchronization of the receiver. Alternatively a long PN code can be used. Long codes are generally thousands to millions of chips in length, thus are only repeated infrequently. Because of this they are useful for added security as they are more difficult to decode.

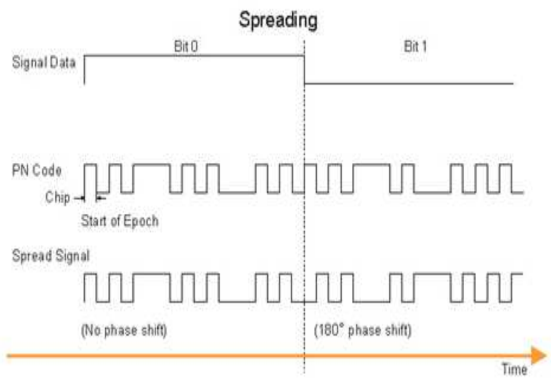

Figure 2.2: Direct Sequence Signals

In DS-CDMA the spreaded signal is modulated by a RF carrier. For the modulation, various modulation techniques can be used, but usually some form of phase shift keying (PSK) like binary phase shift keying (BPSK), differential binary phase shift keying (D-BPSK), quadrature phase shift keying (QPSK), or minimum shift keying (MSK) is employed.

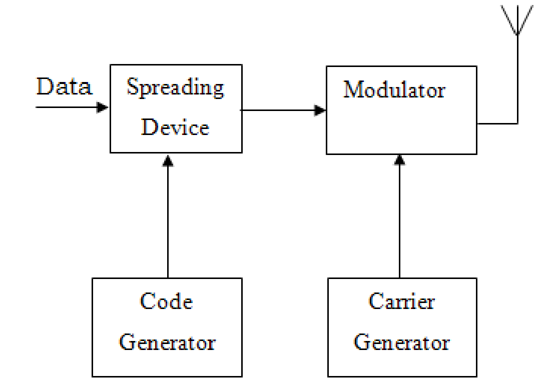

Figure 2.3: Block diagram of CDMA Transmitter

In Direct-Sequence CDMA, the user signal is multiplied by a pseudo-noise code sequence of high bandwidth. This code sequence is also called the chip sequence. The resulting coded signal is transmitted over the radio channel.

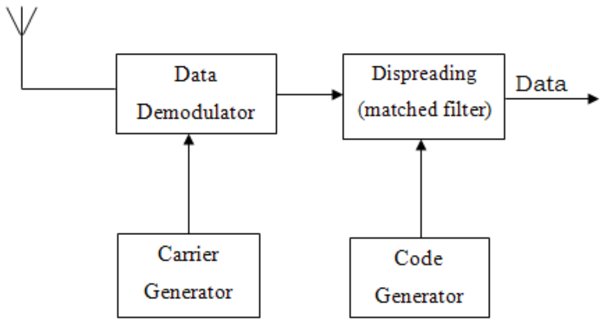

Figure 2.4: Block diagram of CDMA Receiver

After transmission of the signal, the receiver demodulates the received signal and then dispreads the signal using a locally generated code sequence. A Spread Spectrum receiver uses a locally generated replica pseudo noise code and a receiver correlator to separate only the desired coded information from all possible signals. A Spread Spectrum correlator can be thought of as a very special matched filter. It responds only to signals that are encoded with a pseudo noise code that matches its own code. Thus, a Spread Spectrum correlator can be 'tuned' to different codes simply by changing its local code. This correlator does not respond to manmade, natural or artificial noise or interference. It responds only to SS signals with identical matched signal characteristics and encoded with the identical pseudo noise code.

3. Design of CDMA transmitter and receiver

3.1 CDMA COMMUNICATION SYSTEM

CDMA Communication system consists of transmitter and receiver sections along with analog channel. User data is spreaded with the PN Sequence Code at the transmitter and same PN Sequence code is used to dispread at the receiver by using a matched code filter. The most practical, all digital version of Spread Spectrum is direct sequence. A direct sequence system uses a locally generated pseudo noise code to encode digital data to be transmitted. The local code runs at much higher rate than the data rate.

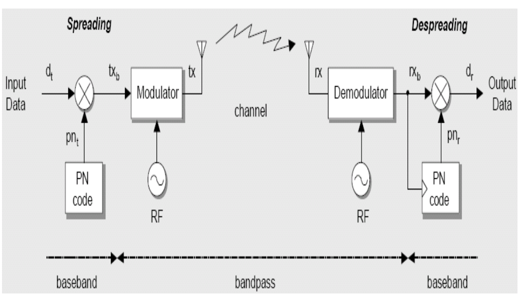

Figure 3.1: CDMA Communication System

In this paper two CDMA communication systems are implemented, one with Maximum Length (ML) sequence PN code and other with gold code. In the PN sequence generator section both the ML sequence and gold code generators are described. The following specifications are considered for design and implementation of the CDMA transmitter and receiver.

3.2 DS-CDMA TRANSMITTER

In CDMA transmission user data is spreaded by a PN sequence and then modulated using BPSK modulation where in the carrier is generated using digital frequency synthesizer principle .Then the modulated signals from different users are combined and transmitted.

The main blocks of CDMA transmitter are listed below:

- Clock distributor
- PN sequence generator
- Signal spreader
- BPSK modulator

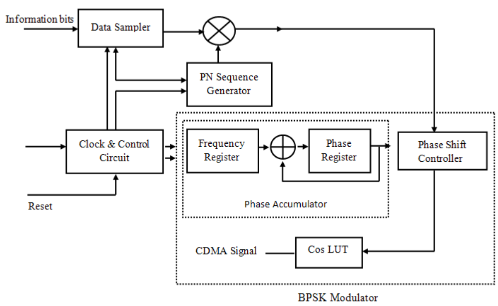

Figure 3.2: Block diagram of DS-CDMA Transmitter

3.3 DS-CDMA RECEIVER

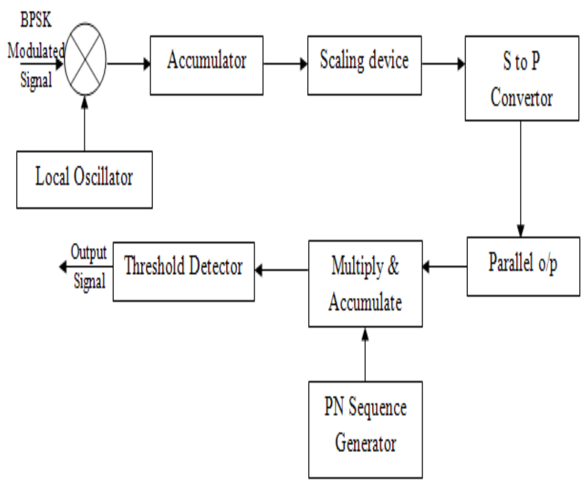

Figure 3.3: Block diagram of DS-CDMA Receiver

The receiver performs the following steps to extract the Information:

- Demodulation
- Accumulation
- Scaling
- Serial to parallel conversion
- Multiplying and dispreading
- Threshold device

4. IMPLEMENTATION OF DESIGN

4.1 VHDL IMPLEMENTATION

VHDL is VHSIC hardware description language common language for designers. This is the high level language and simulation, synthesis tools are available. VHDL supports for versatile design reconfiguration and multiple level of abstraction. A VHDL specification can be executed in order to achieve high level of confidence in its correctness before commencing design and may simulate one to two orders of magnitude faster than a gate level description. A VHDL specification for a part can form the basis for a simulation model to model to verify the operation of the part in the wider system. Behavioral simulation can reduce design time by allowing design problems to detect early on, avoiding the need to rework designs at gate level. Behavioral simulation also permits design optimization by exploiting alternative architectures, resulting better design. VHDL permits technology independent design through support for top down design and logic synthesis.

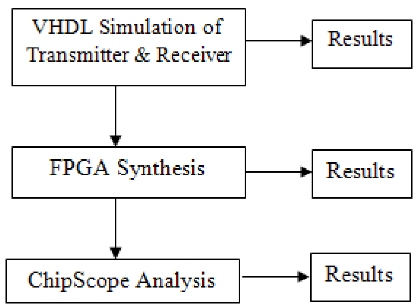

Figure 4.1: DS-CDMA Top Module Implementation Flow

5. RESULTS

5.1 SIMULATION RESULTS

5.1.1 Simulation Result for DS-CDMA Transmitter

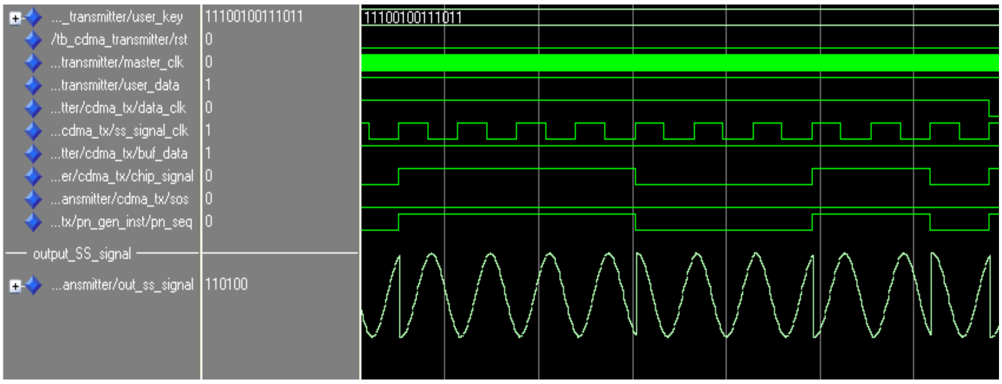

Figure 5.1: Simulation Result for DS-CDMA Transmitter

The above simulation result shows the DS-CDMA transmitter tested with inputs user_key, user_data, pn_seq and output observed is out_ss_signal.

- user key of 14 bits is applied to generate 127 bit gold sequence
- buf_data - it is the user data which is sent to the spreader after buffering so as to maintain synchronization
- pn_seq – it is the generated 127 bit gold sequence which is used for spreading
- sos – it indicates the start of pn_seq when it is 1
- chip_signal – it is the signal obtained after spreading and is same as pn_seq if the buf_data is 1 else it is compliment of the pn_seq
- out_ss_signal – it is the generated DS-CDMA signal

5.1.2 Simulation Result for DS-CDMA Top Module

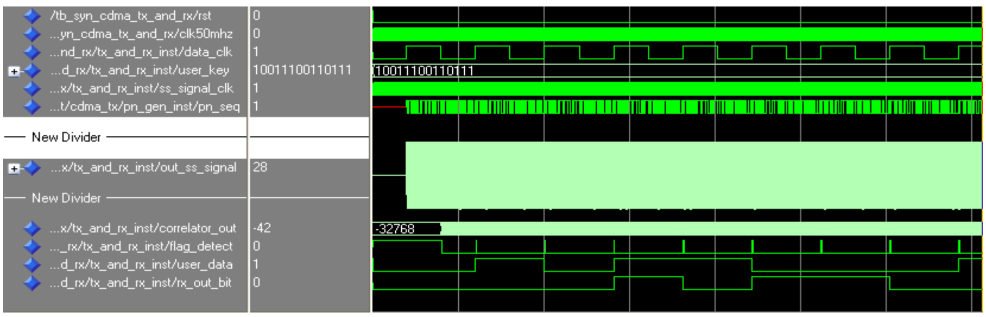

Figure 5.2: Simulation Result for DS-CDMA Top Module

The above simulation result shows the output of the top level module. It can be observed that the received data is same as user data with some amount of delay.

- user key – it is the 14 bit key for the generation of gold sequence
- out_ss_signal – it is the transmitted ds cdma signal
- correlator_out – it is the output of the correlator
- flag_detect – it is raised to 1 whenever a bit is detected. A bit is detected when the correlator output is greater than threshold value
- user_data - -it is the transmitted user data
- rx_out_bit - -it is the received data.

6. CONCLUSION

In the proposed project I have implemented various modules of Direct Sequence Code Division Multiple Access Communication System. It has been observed that the implemented design is fully reconfigurable on any communication links. System developed is implemented with PN-sequence of length 127(Gold code sequence) and it can be implemented with any length sequence very easily.

The developed DS CDMA system provides efficient area utilization on FPGA. This is obtained by implementing scaling process in receiver section. Chipscope analysis which provides testing and on chip debug at runtime is also implemented and the results obtained are satisfactory.

7. References

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