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A PATH FOR HORIZING YOUR INNOVATIVE WORK

DESIGN OF TERNARY NAND GATES USING TERNARY TRANSMISSION GATES

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Abstract: This paper presents Multiple-valued logic gates. The design of 3-valued circuits is a possible substitute of binary logic. While binary logic is limited to only two states, "true" or "false", multiple-valued logic i.e. Ternary logic can replace these with three values in this paper We proposed ternary Nand gates. These gates are used to design simple combinational circuit which is multiplexer with the help of transmission gate. We have shown simulation result of the proposed ternary Nand gate. Also the simulation result shows that proposed ternary Nand gate have very low power dissipation than conventional ternary circuits.

Keywords: Ternary, Ternary AND Gate, Ternary NAND Gate.

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1. INTRODUCTION

Multiple-valued logic (MVL) has in the last few decades been proposed as a possible substitute of binary logic. While binary logic is limited to only two states, "true" or "false", multiple-valued logic (MVL) can replace these with finitely or infinitely numbers of values. A MVL system is defined as a system operating on a higher radix than two [1]. A radix-n set has n elements, 0, 1...n – 1. The practicability of MVL depends on the accessibility of the devices constructed for MVL operations [2]. The devices should be able to switch between the different logical levels, and preferably be less complex than the binary counterpart.

Ternary logic is MVL compliant. However, only three logic states are used, "0", "1" and "2". The optimum radix (r) of a fractional number is found to be the natural logarithm (e). Ternary logic uses number representation with r=3, compared to binary logic which uses r=2, hence the most economical integer radix which is the closest to the natural logarithm e, is base 3 [3].The practicability of MVL depends on the accessibility of the devices constructed for MVL operations.

2. TERNARY INVERTER:

The Yoeli-Rosenfeld algebra [9] we proposed three basic ternary elements the STI (Simple Ternary Inverter), the NTI (Negative Ternary Inverter) and the PTI (Positive Ternary Inverter), whose logic functions are shown in Table To obtained the larger noise and low power dissipation we need to employ a new approach to design a ternary inverter in which there exists a path from each reference voltage to the output.

The three logic levels is employed called as low, middle and high voltage level to the ternary inverter and at a time one logic will active. We used three logic levels 0, 1 and 2 for ternary inverter[9]. The ternary inverter works as a standard ternary inverter. The output is 0 if the input is 2, similarly output are 1 and 2 for input 1 and 0 respectively which is shown in figure 2.

The symbolic representation of the negative ternary inverter (NTI), positive ternary inverter (PTI) and standard ternary inverter (STI) is shown in fig.1.The three basic general type of ternary inverter has one input X and three outputs Y0, Y1 and Y2 which is shown in figure 1[4][5].These types of ternary CMOS inverter have been design.

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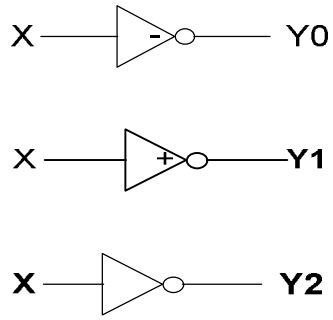

Figure 1: Ternary Inverters (a) Symbol for NTI (b) Symbol for PTI (c) Symbol for STI.

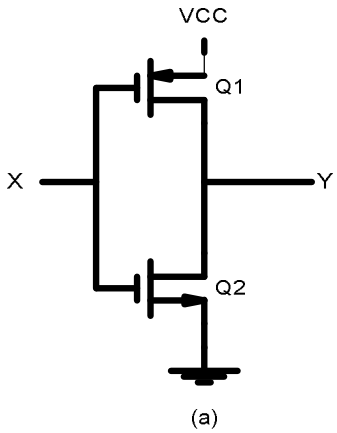

Figure 2: Ternary Inverter

Table 2.1: The rule of ternary inversion

INPUT voltage (X)	OUTPUT voltage)
0	1
1/2	½
1	0

3. TERNARY AND GATE:

A TAND function gives the minimum value of the input signal where Input signal belongs to 0, 1/2 and 1. The design of TAND gate is shown in figure 5 it is designed by connecting the combination of two CMOS transmission gate namely TG1 and TG2 as shown in figure 2.The truth table of TNAND is given in table. The operation of the TNAND gate can be understood easily.

The control signal input i.e.Vin1 and Vin2 is given to the bottom and top TGs respectively. If the control signals input Vin2 is logic high for the input Vin1 0, 1/2 and 1, then the top TG will be conduct and the output will be equal to the input Vin1. If the control signals input vin2 is low, then the top TG will be off and the output is 0. When the control signal input Vin2 is 1/2 i.e. middle, then top TG is on and the output is equal to control signal input vin1 except vin1 is logic high. When control signal input Vin1 is high, then bottom TG will be conduct and output will be equal to control signal input Vin2. The new proposed implementations of the TAND gate which has very low static power dissipation. Many ternary logic models exist in the literature, but they generally involve high power consumption [6][7][10] As we know that, transmission gate is used as a switch. To design a TAND, we make the used conventional design of transmission gate [4][5].

The CMOS implementation of transmission gate is shown in figure 4. The N-MOS switch is open if control signal of the N-MOS switch is 0 and is closed if control signal of the N-MOS switch is 1 shown in fig. 4.Similarly for P-MOS switch of is open if control signal of the P-MOS is 1 and is closed if control signal of P-MOS is 0 shown in fig 4.

The input of the P-MOS and N-MOS is denoted as C and C bar which is shown in figure 4. The input to both is available through the binary inverter. If the input of the inverter is 1 and inverted output $\bar{C}$ is 0 then **C** and C bar are given to N-MOS and P-MOS switch respectively which is shown in figure. If the input of the inverter is 0 and inverted output $\bar{C}$ is 1 then C and $\bar{C}$ are given to N-MOS and P-MOS switch respectively which is shown in figure 4[4]

The truth tables for the TAND are given in Table 3.1

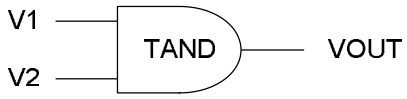

Figure 3: Symbol for TAND Gate.

TABLE 3.1

V1	V2	V1 TAND V2
0	0	0
½	0	0
1	0	0
0	½	0
½	½	½
1	½	½
0	1	0
½	1	½
1	1	1

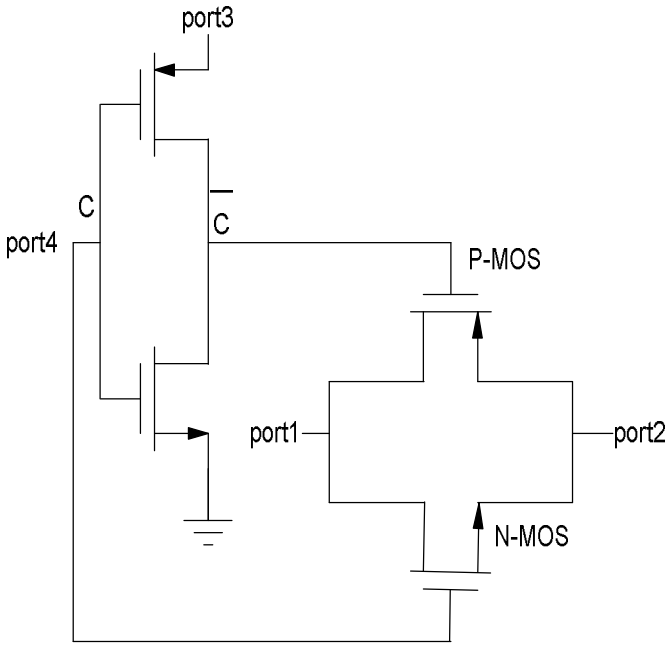

Figure 4: Ternary transmission gate

[4]. after applying ternary input to transmission gate, output is taken at port 2 that is Vout. To port 3 I_PROBE is connected to measure the power dissipation. This new proposed implementations of TAND have very low static power dissipation measure by the I_PROBE.The operation multiplication which can be called Ternary AND (TAND) represent two multiple input operators. It is represented by following equations

V1,V2,V3,…….VN.=MIN(V1,V2,V3,…VN) Eq.(1)

3. PROPOSED TERNARY NAND GATE:

A TNAND function gives the minimum value of the input signal where input signal belongs to 0, 1/2 and 1. The TNAND gate is shown in figure 8[8]. The design of TNAND gate consists of three transmission gates.

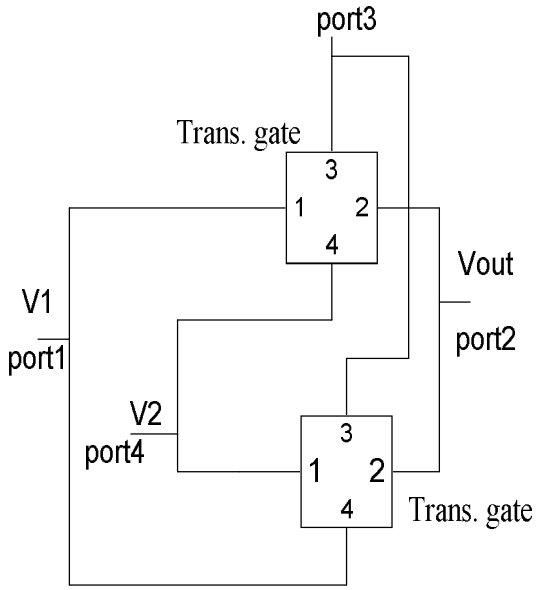

Figure 5: Ternary AND gate

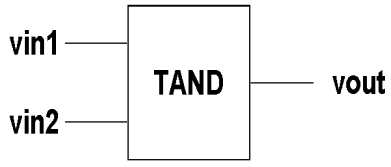

Figure 6: Block diagram of TAND gate

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Truth table 4.1: Ternary NAND gate

Vin1	Vin2	Vin1 TNAND Vin2
0	0	1
0	1/2	1
0	1	1
1/2	0	1
1/2	1/2	½
1/2	1	0
1	0	1
1	1/2	½
1	1	0

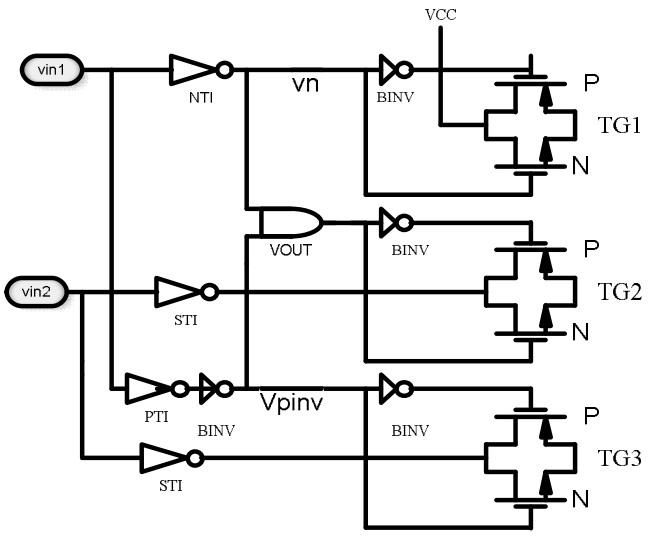

Figure 8: Block diagram of Ternary NAND gate

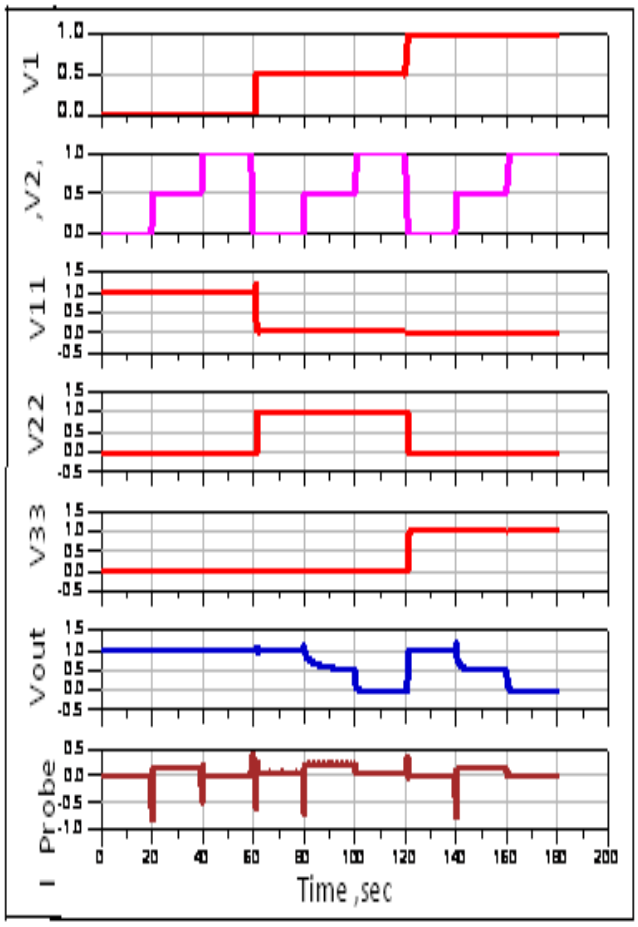

Figure 9: Simulation result of Ternary Nand gate

5. CONCLUSION:

In this paper I have design ternary NAND gate which has very low power dissipation as compared to conventional ternary NAND gate. The proposed ternary NAND gate is used to design combinational circuits.

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