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A PATH FOR HORIZING YOUR INNOVATIVE WORK

DESIGN CMOS LOW NOISE AMPLIFIER FOR 2.47 GHZ FREQUENCY AT 0.18MM TECHNOLOGY

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Abstract: The objective is to develop an amplifier with desired specifications. In this paper we have tried to explain how we designed an amplifier at 2.47 GHz for W-LAN application and had two options. They were whether to design a power amplifier (PA) or to design a low noise amplifier (LNA). The possibility of PA was eliminated by the fact that we were going to use it as the first block in receiver side. Hence it had to be a LNA. We are using 0.18µm technology for designing purpose. So our length is fixed to 0.18µm and to obtain the desired value of current, width is to be varied. Value of current, in IC designing, depends on the ratio of width (W) and length (L). We used "ADVANCED DESIGN SYSTEM" for simulation purpose. It is user friendly tool and easy to understand. ADS is the *"Hi-Frequency & Hi-Speed" platform for IC, Package and Board Co-Design.*

Keywords: Advanced design system, Low noise amplifier, Input and output matching, RFIC, VLSI

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INTRODUCTION

A low noise amplifier (LNA) requirement is important with regard to system performance due to growth of modern communication systems [1-3].Amplification is one of the most basic and prevalent RF circuit functions in modern RF and microwave systems. To amplify the received signal in a RF system, a low noise amplifier (LNA) is required. The goal of this is to design an LNA with lowest noise figure possible, with gain as high as possible.

First stage of a receiver is typically a low noise amplifier (LNA), whose main function is to provide enough gain to overcome the noise of subsequent stages [4]. Aside from providing this gain while adding as little noise as possible, an LNA should accommodate large signal without distortion and frequently must also prevent specific impedance, such as 50Ω, to the input source. We have used an inductive source degenerated LNA topology for the application in WCDMA have minimum noise figure [5].

To develop a design strategy that balances gain, input impedance, noise figure and power consumption, we will derive analytical expressions for the four noise parameters directly from device noise model and will then examine several LNA architectures. From this, we will design a LNA with near minimum noise figure, along with excellent impedance match and good power gain.

The Low Noise Amplifier (LNA) always operates in Class A, typically at 15-20% of its maximum useful current. Class A is characterized by a bias point more or less at the center of maximum current and voltage capability of the device used, and by RF current and voltages that are sufficiently small relative to the bias point that the bias point does not shift.

The LNA function, play an important role in the receiver designs. Its main function is to amplify extremely low signals without adding noise, thus preserving the required Signal-to-Noise Ratio (SNR) of the system at extremely low power levels.

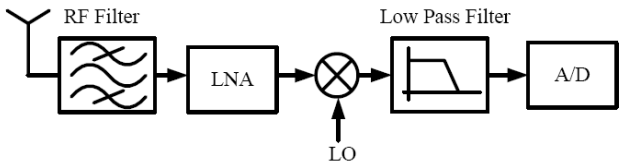


Figure 1.1: RF receiver

It is known that the LNA is the first active amplification block in the receiving path as shown in Figure 1.1. In fact, the performance of the RF receiver is significantly influenced by the LNA. Being the first block of the receiver, the LNA plays a crucial role in amplifying the received signal while adding little noise to it. In addition, the input of the LNA needs to be matched to the output of the filter following the antenna to prevent the incoming signal from reflecting back and forth between the LNA and the antenna. While the LNA is a relatively simple design compared to other RF components in a cellular receiver chain, the performance tradeoffs challenge the LNA design engineer. LNA design typically involves making choices between directly competing performance parameters such as: noise, gain, linearity and power consumption.

II. IEEE Standard (802.11b) WLAN

The Institute of Electrical and Electronics Engineers (IEEE) created the WLAN 802.11(b) standard in Sept. 1999. Standard 802.11(b) supports the bandwidth up to 11 Mbps. These have lowest cost, signal range is 35 meter indoor and 140 meter outdoor. Table I summarizes the important specification of WLAN standards 802.11(b).

Parameter	IEEE Standard 802.11(b)
Release	Sept. 1999
Frequency Range	2400-2483 MHz
Max. data rate	11 Mbps / 5.5 Mbps
Modulation	DSSS
Indoor range	35 meter
Output range	140 meter

Table I Summarized WLAN 802.11 (b) Standards

III. LNA Circuit Design

The complete circuit of LNA can be designed by using three sections this are given below

1. Input matching network

2. Main transistor section

3. Output matching network

The input matching network is used to make the input return loss (S11) minimized without introducing additional noise. The input matching circuit that terminates the transistor to gamma optimum (Γout) which represents the input impedance of the transistor for the best noise matches. Main transistor section ensures a high gain, high linearity and low noise factor at the time of input and output matching. The last step in LNA design involves output matching. The input and output impedance matching is required to maximize the power transfer and minimize the reflections. Smith chart is used for impedance matching. According to maximum power transfer theorem, maximum power delivered to the load when the impedance of load is equal to the complex conjugate of the impedance of source (ZS = ZL*).

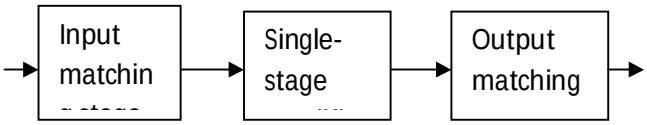


Fig.2 Low noise amplifier structure

LNA structure consists of input matching stage, single stage amplifier and output matching stage. In this paper, we use the inductively degenerated common source topology as shown in figure 3.

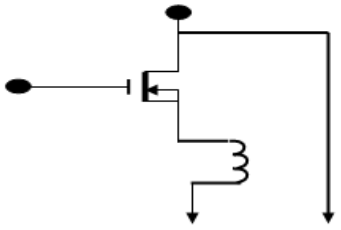


Fig.3 Inductive source degeneration

This topology has been best choice for many frequency bands due to its noise and gain performance. Input matching (S11) can be improved by the use of changing the source

degeneration. Through a choice of inductance L_s, control over the real part of the input impedance can be obtained. From the small signal equivalent of this circuit (Fig. 3-I), the input impedance can be computed as follows.

$$V_x = \frac{I_x}{j\omega C_{gs}} + j\omega L_s (I_x + g_m V_{gs})$$

(3-1)

$$\frac{V_x}{I_x} = Z(j\omega) = \frac{1}{j\omega C_{gs}} + j\omega L_s + g_m \frac{L_s}{C_{gs}}$$

(3-2)

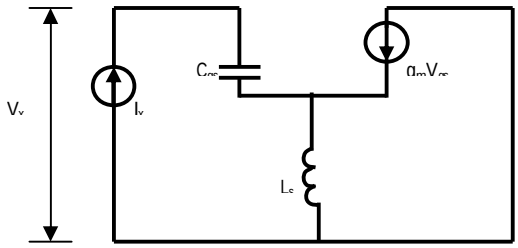


Fig. 3-I Small signal model

Hence, the input impedance of a series RLC network, with a resistive term that is directly proportional to the inductance value. Also, L_s does not bring with it the thermal noise of an ordinary resistor because a pure reactance is noiseless. This property can be exploited to give specified input impedance without degrading the noise performance of the amplifier. This input impedance is purely resistive at only one frequency (at resonance), however, so this method can only provide a narrow band impedance match, which is suitable for the current design. Hence, a method that creates a real part of input impedance without additional noise is found.

IV. Methodology

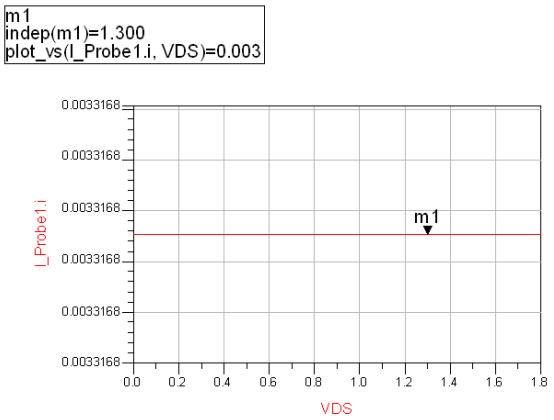
A. Selection of MOS Transistor

This is the first and the most important step while designing an on chip LOW NOISE AMPLIFIER. The selection of MOS depends on its mobility, so we have selected an enhancement type of n-MOS transistor. The three important parameters in the transistor are V_{ds}, V_{gs} and I_{ds}.

Values of V_{ds} and V_{gs} are predetermined. We have to obtain the desired value of Ids which is dependent on W/L ratio of MOS transistor. Since we are using 0.18µm technology, our device length is fixed at 0.18 micrometer. The only parameter on which the Ids depend is "width" of the device.

$$I_{ds} = \left[\frac{\mu n \cdot Cox}{2}\right] * \left[\frac{W}{L}\right] * (V_{gs} - V_t)^2$$

Values of μ_n and C_{ox} are dependent on fabrication process. Since we are using 0.18µm technology C_{ox} = 8.42 fF. For simulation purpose we are using BSIM 3 model, hence the device width is reduced by 20% to 30% of the calculated width.

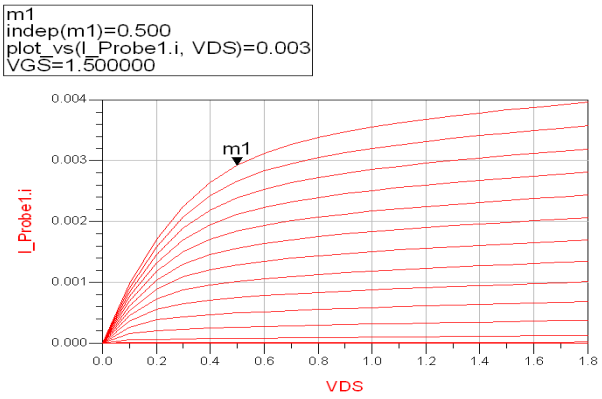


B. DC Simulation

Biasing in electronics is the method of establishing predetermined voltages or currents at various points of an electronic circuit to set an appropriate operating point. The operating point of a device, also known as bias point, quiescent point, or Q-point, is the steady-state operating condition of an active device (a transistor or vacuum tube) with no input signal applied.

The importance of DC simulation is to determine the quiescent point of the device MOS. The DC Simulation controller calculates the DC operating characteristics of a design under test (DUT). Fundamental to all RF/Analog simulations, DC analysis is used on all RF/Analog designs.

- DC Simulation Result



C. Feedback Network Design

Feedback can be either negative or positive. In amplifier design, negative feedback is applied to affect the following properties.

1. Desensitize the gain
2. Reduce non-linear distortion
3. Reduce the effect of noise
4. Control the input and output impedan

D. S Parameter

Scattering parameters are all about power; both reflected and an incident in a linear two port system. It assumes that the system must be treated like a transmission line system. It is refers to RF output voltage verses input voltage in the RFIC and describes the relationship between the two or more port network. In the term of RFIC, S11and S22 is called reflections

Coefficient S21 and S12 are called transmission coefficient. S11 and S22 are used to calculate the input and output reflection in the circuits [23]. S21 and S12 are used to calculate the forward and reverse voltage gain in dB as shown in the figure 4.

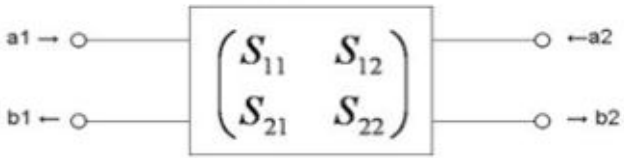


Figure 4: S Parameter Two Port Model

E. Noise Figure

Besides stability and gain, another important design consideration for a microwave amplifier is its noise figure. In receiver applications, it is often required to have a preamplifier with as low a noise figure as possible, as the first stage of a receiver front end has the dominant effect on the noise performance of the overall system. The noise figure parameter, N, are given where, the quantities F_{min}, Γ_{opt} and R_N are the characteristics of the transistor being used and are called the noise parameters of the device.

It is the ratio of output SNR to the input SNR in dB:

$$NF\ (dB) = 10\log \frac{SNR_O}{SNRi}$$

F. Impedance Matching

The impedance matching network is lossless and is placed between the input source and the device. The need for matching network arises because amplifiers, in order to deliver maximum power to a load, or to perform in a certain desired way must be properly terminated at both the input and the output ports. The impedance matching networks can be either designed mathematically or graphically with the aid of Smith Chart. Several types of matching networks are available, but the one used in this design is open single stubs whose length is found by matching done using smith chart manual.we have managed to match impedance with the terminating resistance of 50 Ω. Γs and ΓL is the source and load reflection coefficient respectively. Input and output reflection coefficient is Γin and Γout respectively shown in following equations:

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}$$

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_s}$$

G. Linearity

Linearity of LNA is most important in a wireless receiver to reduce the inter-modulation distortion. The linearity is expressed by the 1 dB compression point and inter-modulation product (IP3). When the input signal is increased, a point is reached where the power of the signal is not amplified by the same amount as the smaller signal at the output. At this point where the input signal is amplified by an amount 1 dB less than the small signal gain, these are called 1 dB compression point.

V. Experimental Discussion

The design and simulation of an inductively degenerated CMOS Low Noise Amplifier (LNA) is presented operating at 2.47 GHz. The LNA has a noise factor less the 2dB and a forward gain greater than 13 dB with actual chip parasitic and gate noise modeled. This design was completed in 0.18µm technology with a 1.8V supply. The input and output power matches are better than -12 dB.

While designing the schematic, following are the observations made:

- An LNA design presents a considerable challenge because of its simultaneous requirement for high gain, low noise figure, good input and output matching and unconditional stability at the lowest possible current draw from the amplifier.

- Although Gain, Noise Figure, Stability, Linearity and input and output match are all equally important, they are interdependent and do not always work in each other's favor.

- Carefully selecting a CMOS transistor and understanding parameter trade-offs can meet most of these conditions.

- Selection of CMOS is the first and most important step in an LNA design. The designer should carefully review the transistor selection, keeping the most important LNA design trade-offs in mind.

VI. Expected Outcome and Future Work

In this project the Low Noise Amplifier will be design and will meet the following specification

1. Frequency : 2.47GHz

2. Gain more than 13dB

3. Supply Voltage : 1.8V

4. Noise figure near about 0.5 dB.

5. Drain Current : 3Ma

We have not achieved desired results in the two stage amplifier apart from its gain. The improvement of this two stage LNA is still in research process to achieve the desired results and is a part of our project extension.

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