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DESIGN AND ANALYSIS OF GATE-STACK DOPING-LESS TUNNEL FIELD EFFECT TRANSISTOR

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Abstract: In this paper, a Gate-stack Doping-less Tunnel field effect transistor is proposed using a double- gate doping-less TFET(DLTFET) with a multilayer gate-stack architecture. The device characteristics are demonstrated and compared with DLTFET. It is found that the proposed architecture is having better performance than DLTFET. It is based on Charge plasma concept. There is no Source and Drain doping applied. Thus, it is free from Random dopant fluctuation issue and highly reliable. The gate dielectrics are used in stack manner to form a multilayer architecture. It provides the ON current of about 0.1 mA/µm with a low OFF current, 5×10^{-18} A/µm. The threshold voltage is 0.8V and the Sub-threshold swing is calculated as 77mV/dec. All the simulations has been performed using SILVACO ATLAS device simulator.

Keywords: Charge-plasma, Doping-less, Gate-stack, Random Dopant fluctuations, Work function.

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INTRODUCTION

A conventional MOSFET having Sub-threshold Swing limitation has put barrier to further scale the power supply voltage. Tunnel FET (TFET) has overcome this limitation of conventional MOSFET [1],[2] which is based on band-to-band tunneling(BTBT) mechanism, thus enabling the power supply Scaling[3] and make it fit for ultra-low power applications. TFET has many other advantages over MOSFET[4],[5], such as more immunity to short channel effects, high speed operation, smaller threshold voltage roll-off, low OFF-state current. One of the significant problems with TFET is the Random dopant fluctuations (RDF) which results in variations in transistor performance [6]. There is large increase in OFF-state current due to RDF [7]-[10]. A very abrupt source and drain junctions are necessary for better tunneling. But it requires a high thermal budget and complex annealing techniques [11]-[13]. Doping-less TFET (DLTFET) which does not require any doping in the source and drain regions, is free from RDF issues resulting in better reliability [14]. It is having a charge plasma phenomenon, in which the p+ source and n+ drain regions are formed by using the source and drain metal electrodes having appropriate work functions[15]-[17]. It requires low thermal budget. However, DLTFET suffers from low ON-state current and high sub-threshold swing due to poor band-to-band tunneling efficiency.

Various methods has been reported to improve the ON-state current such as a double gate architecture[18], the use of SiGe [19],[20] at the source side, III-V[21]-[25] heterostructures , use of source pocket

doping[26] , a high-k dielectric[18],[27], a thin silicon body[28], a low-k spacer[29], band-gap engineering[30]. One of the simplest and efficient method is multilayer Stacked architechture of dielectrics on gate[31]. It consists of a thin Silicon-di-oxide layer between the Silicon body and high-k dielectric.

Combining the advantage of high reliability of Doping-less and the advantage of good ON-state current with low sub-threshold swing of Gate-Stack, we propose a new device that is Gate-stack Doping-less Tunnel field effect transistor (GS-DLTFET).

The contents of the paper are organized as follows: Section II describes the device structure under investigation and setup for the simulation. Section III presents the impact of scaling, impact of drain voltage on device characteristics, impact of gate voltage on output characteristics and energy band diagrams.

I. Device Structure and Simulation

In this section, the device structure and simulation procedure are explained. The simulated n-type GS-DLTFET structure is shown in Fig. 1. ATLAS device simulator is used for simulation. The channel length (L) of the device is taken as 50nm. The intrinsic carrier concentration, $n_i = 1.0 \times 10^{15} / cm^3$.

The Silicon body thickness (t_{Si}) used here is 10nm. The lower gate-oxide thickness (high-k dielectric) is 2nm. The gate metal work function is taken as 4.5eV.

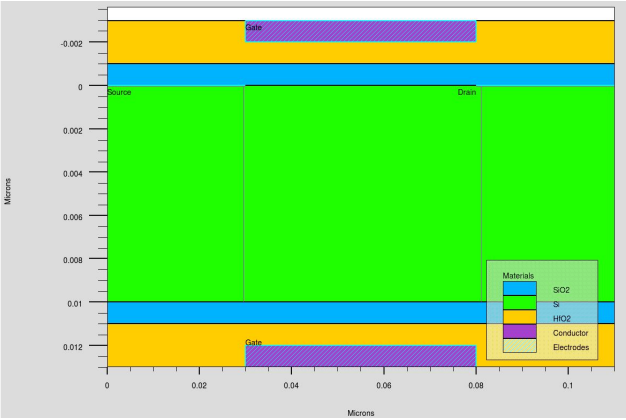

Figure1. Structure of Gate-stack doping-less TFET

In this structure, the p+ source and n+ drain regions are formed using a phenomenon of charge plasma. The drain metal electrode used here is hafnium having low work function of 3.9eV, which induces electrons in the drain region to form it n-type. Similarly, the source metal electrode used is platinum having low work function of 5.93eV, which induces holes in the source region to form it p-type.

The models used for device simulations are non-local band-to-band tunneling (BTBT) model, recombination model CONSRH (concentration dependent Shockley Read Hall recombination), CVT (Lombardi mobility model).

II. RESULTS AND DISCUSSION

Figure2 shows the I_D-V_{GS} characteristics of the GS-DLTFET at V_{DS}=1.6V and its comparison with the DLTFET. The ON-state current for the new structure has improved to 0.1mA/µm with a low OFF-state current of 5×10^{-18} A/µm as compared to the DLTFET. The threshold voltage is found

to be 0.8V by constant current method (the value of V_{GS} at which drain current becomes 1×10^{-7} A/μm). The average sub-threshold swing is calculated to be 77mV/decade.

Figure3 shows the effect of technology scaling on I_D-V_{DS} characteristics. The plot depicts the transfer characteristics for four different values of gate length (L), namely, 20, 30, 40, 50nm. It is clear from the figure that there is no impact of technology scaling on the device characteristics as they seem to be almost same.

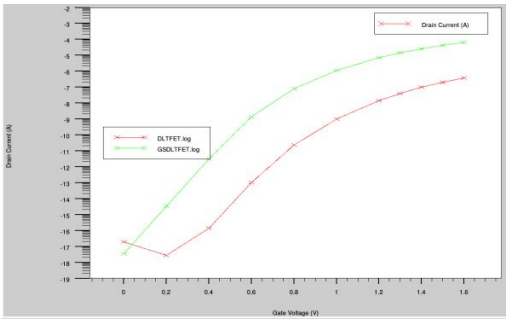

Figure2. I_D-V_{GS} characteristics curve of the GS-DLTFET at V_{DS}=1.6V and its comparison with the DLTFET.

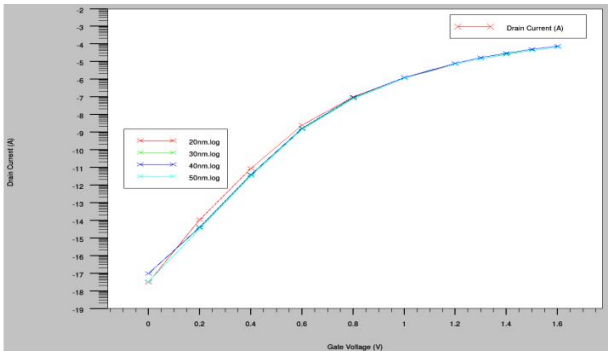

Figure3. Impact of technology scaling on I_D-V_{DS} characteristics Figure4 presents the transfer characteristics for different values of V_{DS}. It is evident in the figure that there is an increase in the ON-state current with a slight change in the OFF-state current by increasing the value of drain voltage. The output characteristics for different values of V_{GS} are plotted in Fig. 5. A perfect saturation can be clearly seen from the figure. Also, it is noticed that for V_{DS} value greater than the pinch off voltage i.e. 0.2V here, drain current becomes constant and less dependent on V_{DS}.

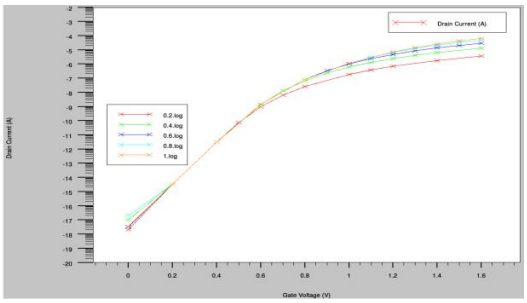

Figure4. Transfer characteristics for different values of V_{DS}.

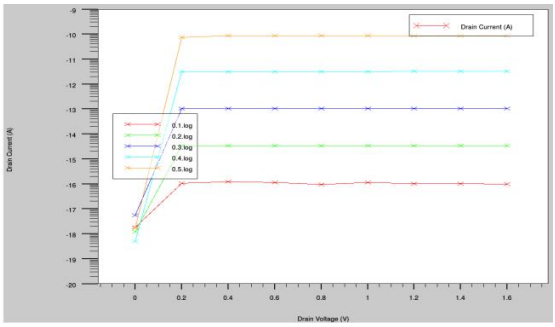

Figure5. The output characteristics for different values of V_{GS}

Figure6 shows the simulated energy band diagrams at 1nm below the Silicon-di-oxide and semiconductor interface, for different values of V_{DS} at V_{GS}=1V. It is shown that the tunneling width goes on reducing with increase in the value of V_{DS}, which in turn increases the drain current.

The energy band-diagrams along the two horizontal cutlines has been plotted at V_{GS}=1V and V_{DS}=1.5V in Fig. 7. The first cutline is at 1nm below the Si-SiO2 interface and the other at the middle of the Silicon body. It is observed that the tunneling width at 1nm depth is less as compared at the middle. This is due to the reduction in carrier concentration along the thickness of the Silicon body, as the metal electrodes responsible for generating the free carriers are present only on the top side of the Silicon film.

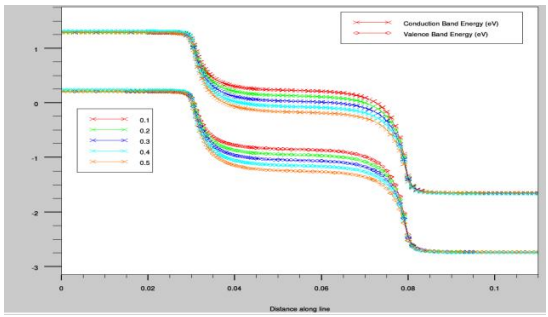

Figure6. Energy band diagrams at 1nm below the SiO2 and Silicon interface, for different values of V_{DS} at V_{GS}=1V.

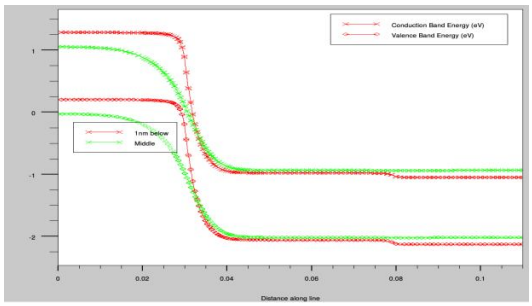

Figure7. Energy band-diagrams along the two horizontal cutlines at V_{GS}=1V and V_{DS}=1.5V

IV. CONCLUSION

In this paper, a new TFET architecture has been proposed named as Gate-stack doping-less Tunnel FET. We have presented a simulation study of the device and its characteristics. Our simulation results show that the device is having good ON-state current with a very low OFF-state current. The value of Sub-threshold swing is found to be low. As there is no doping in source and drain regions, there is no issue of Random dopant fluctuations resulting in high reliability. It also reveals that there is no impact of scaling the gate length on the device characteristics. The drain current is dependent on drain voltage as it increases with the increase in drain voltage. The charge concentration decreases along the thickness of the device.

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