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VLSI ARCHITECTURE FOR OPTIMIZED LOW POWER DIGIT SERIAL FIR FILTER WITH FPGA

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Abstract: In the last two decades, many efficient algorithms and architectures have been introduced for the design of low power FIR Filter which dominates the complexity of many digital signal processing systems. On the other hand, little attention has been given to the digit-serial design that offers alternative low complexity since digit-serial operators occupy less area and are independent of the data word length and low power operations at the cost of an increased delay. In this topic, we address the problem of optimizing the area in multiple constant multiplier and digit serial adder, design architectures. The proposed optimization algorithms for the digit-serial architecture is used in the design of digit-serial finite impulse response filters that will yield better performance, with high efficiency.

Keywords: Digit Serial Adder, Fir filter, MCM, Optimum Area, Power, Shift and Add Adder.

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INTRODUCTION

It is well known that bit-serial systems, which process one bit of the input sample in one clock-cycle, for area efficient and ideal for low-speed applications [1]. On the other hand bit-parallel systems, which process one whole word of the input sample in one clock cycle, are ideal for high-speed applications [2]. However, in applications which require moderate sample rates, both these systems may be ineffective. Bit-serial systems may be too slow and bit-parallel systems may be faster than necessary and occupy considerable amount of area. To this end, digit-serial systems [3][4] have become attractive for digital designers in the recent past.

These systems process multiple bits of the input word, referred to as the digit size, in one clock cycle. For a digit size of unity, the system reduces to a bit-serial system and for a digit size equal to the word length; the system reduces to a bit-parallel system. Most of the DSP computations involve the use of multiply–accumulate operations, and therefore the design of fast and efficient multipliers is imperative. Moreover, DSP architectures have in need of low-power designs [5] causes the batteries life. Design of digit-serial architectures which can be pipelined at the bit-level [6]. The advantage of digit serial architectures is processing n speeds options, less area and critical path is reduced.

A systematic design methodology for low power digit-serial multipliers is presented.

Filter implementation has concentrated on implementation using various VLSI technologies. Finite Impulse Response (FIR) filters are of great importance in Digital Signal Processing (DSP) systems since their characteristics in linear-phase and feed-forward implementations make them very useful for building stable high-performance filters. The direct and transposed-form FIR filter implementations are illustrated in Fig. 1(a) and (b), respectively. Although both architectures have similar complexity in hardware, the transposed form is generally preferred because of its higher performance and power efficiency [1]. The multiplier block of the digital FIR filter in its transposed form [Fig. 1(b)], where the multiplication of filter coefficients with the filter input is realized, has significant impact on the complexity and performance of the design because a large number of constant multiplications are required and is also a central operation that has performance bottleneck in many other DSP systems such as fast Fourier Transforms, Discrete Cosine Transforms (DCTs), and error-correcting codes. In several cases it is senseless to use conventional bit-parallel circuits: their implementations have an important cost in area and run faster than the speed needed by the application. In this way, digit-serial architectures become an important alternative to efficiently implement a wide range of real time signal processing circuits. The digit-serial approach allows the designer to select an intermediate area-

time, situated between the bit-parallel and the bit-serial implementations. However, the digit-based recoding technique does not exploit the sharing of common partial products, which allows great reductions in the number of operations and, consequently, in area and power dissipation of the MCM design at the gate level. Hence, the fundamental optimization problem, called the MCM problem, is defined as finding the minimum number of addition and subtraction operations that implement the constant multiplications. Note that, in bit-parallel design of constant multiplications, shifts can be realized using only wires in hardware without representing any area cost.

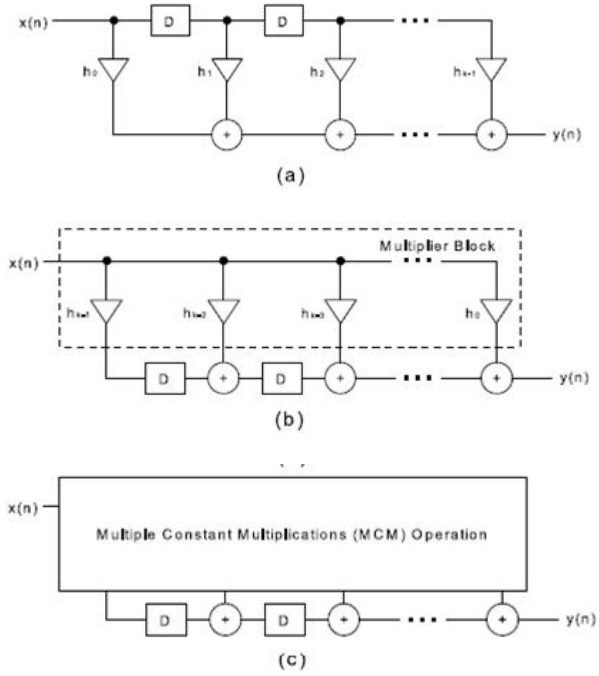

Fig. 1:FIR filters implementations. (a) Direct form. (b) Transposed form with generic multipliers. (c) Transposed form with an MCM block.

LITERATURE REVIEW

1. An Algorithm for the Design of Low-Power Hardware-Efficient FIR Filters-2008[7]

Mustafa Aktan, Arda Yurdakul, and Günhan Dündar, *Member, IEEE.*

This algorithm optimizes SPT terms in the coefficients given the filter frequency-response characteristics. Although the worst case run-time of the algorithm is exponential. The filters

found by the proposed algorithm have fewer SPT terms and are shorter in word length than the filters found by the other methods.

2. Design and Implementation of Low Power Digital FIR Filter based on low power multipliers and adders on xilinx FPGA -2011[8]

Bahram Rashidi Bahman Rashidi Majid Pourormazd

This paper presents the methods to reduce dynamic power consumption of a digital Finite Impulse Response (FIR) filter these methods include low power serial multiplier and serial adder, combinational booth multiplier,folding transformation in linear phase architecture and applied to fir filters to reduce power consumption.

3. Systematic Design of High-Speed and Low-Power Digit-Serial Multipliers – 1998[9]

Yun-Nan Chang , Janardhan H. Satyanarayana, Keshab K. Parhi.

These architectures can be pipelined at the bit-level, and as a result power can be reduced. The power consumed by a bit-serial design due to high-speed clock is much higher and this favors digit serial architectures with respect to low power consumption. Comparison of critical path and power consumption of different digit-serial multipliers and their variation with respect to digit sizes have been explored

4. Design of Digit-Serial FIR Filters: Algorithms, Architectures, and a CAD Tool -2013[10]

Khader Mohammad, Sos Agaian

In this paper, we introduced the 0–1 ILP formalization for designing digit-serial MCM operation with optimal area at the gate level. They also proposed an approximate GBalgorithm that finds the best partial products in each iteration which yield the optimal gate-level area in digit-serial MCM design.

5. Low Power Implementation of Decimation Filters in Multistandard Radio Receiver Using Optimized Multiplication-Accumulation Unit -2007[12]

Nadia Khouja, Khaled Grati, Adel Ghaze

In this work, the implementation of decimation filters for multistandard wireless transceivers was optimized to reduce its power consumption. The power reduction is achieved through the usage of a MAC unit inside the filters that reduce the total activity and therefore the dynamic power. The multiplication function of the MAC unit is based on the Radix-4 modified-Booth

algorithm for the generation of the partial products. For summation, carry save addition was used. A Pipeline stage is then introduced.

PROPOSED ARCHITETURE:

The designing digit serial arithmetic operation with optimal area at the gate level by considering the implementation cost of digit serial addition, subtraction and shift operation is one of the most important parameter. Realization of digit-serial FIR filters under the shift-adds architecture for area reduction compare to the filter designs whose multiplier blocks using digit-serial constant multipliers and power reduce by using the high-level optimization algorithms is proposed here by Digit-Serial FIR Filter.

PROPOSED ALGORITHM:

Digit serial FIR Filter for low power can be designed using 1.Digit Serial Adder Figure shows the Digit-serial architecture for word length of 4 (W=4). This adder adds two four digit numbers x3x2x1x0 and y3y2y1y0 to get 4 digit sum s3s2s1s0 where bit 0 is the least significant bit and bit 3 is the most significant bit. Initially cin=0, we have to kept cin=0 using switch, after it we force full-adder with data x0y0 we get the value of sum s0. For next iteration we connect cout to cin using switch and we force the full-adder x1y1 we get the value of s1 and so on.

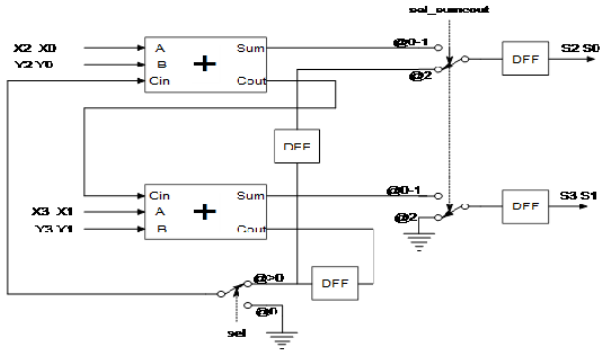

Fig. 2:Digit Serial Adder

2.Multiple Constant Multiplier with Shift and Add algorithm

Multiplication of a variable with a set of constants, known also as the MCM operation, is a central operation and performance in many DSP applications such as, error correcting codes, linear DSP transforms, and Finite Impulse Response (FIR) filters.In hardware, the multiplication operation is considered to be expensive, as it occupies significant area. Hence, constant

multiplications are generally realized using addition, subtraction, and shift operations. Shifts can be implemented using only wires in hardware.

Consider The Constant Multiplication 29x and 43x

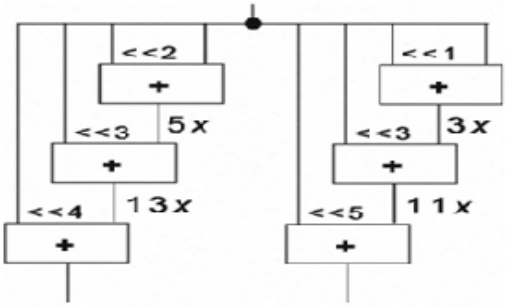

Fig3(a): Without Partial Sharing

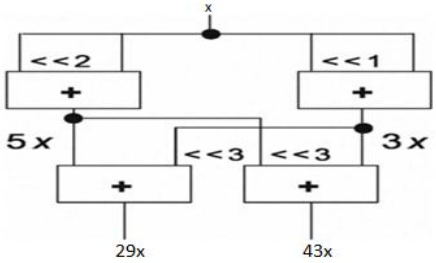

Fig3(b): With partial product sharing

CONCLUSION:

A Transposed form FIR filter using Digit Serial Adder and MCM with shift and add technique can be designed to reduce the complexity and area. Proposed optimization algorithms for the digit-serial architectures in the design of digit-serial operations and finite impulse response filters yield better performance, with high efficiency. In future, this can be implemented on analog tools which give more specified results as per power & many other parameters. By varying the parameters further reduction in the power consumption may be possible.

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