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A PATH FOR HORIZING YOUR INNOVATIVE WORK

PARALLEL ARRAY MULTIPLIER DESIGN TECHNIQUES

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Abstract: Power management has become a great concern in VLSI design in recent years. It is well know that multiplier consumes most of the power in Digital signal processing computations it is very important for modern Digital signal processing system to design low power multipliers to reduce power. This paper explores the design techniques of multiplier and aims to reduce power consumption. Here the bypassing techniques are used to reduce power consumption.

Keywords: RF: Low Power, Power Consumption, Array Multiplier, Column Bypassing, Row Bypassing,

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INTRODUCTION

Multiplication is the basic building block for several DSP processors, Image processing and many other. Over the years the computational complexities of algorithms used in Digital Signal Processors (DSPs) have gradually increased. This requires a parallel array multiplier to achieve high execution speed or to meet the performance demands.

A typical implementation of such an array multiplier is Braun design. Braun multiplier is a type of parallel array multiplier [1].

In DSP applications, most of the power is consumed by the multipliers. Hence, low power multipliers must be designed in order to reduce the power dissipation in DSP applications .The dynamic power of the multiplier can be reduce by using bypassing techniques [1].

As the scale of integration keeps growing, more and more sophisticated signal processing systems are being implemented on a VLSI chip. These signal processing applications not only demand great computation capacity but also consume considerable amounts of energy. While performance and area remain to be two major design goals, power consumption has become a critical concern in today's VLSI system design.

Multipliers have large area, long latency and consume considerable power. Therefore, low-power multiplier design has been an important part in low-power VLSI system design.

1.1) Power consumption

CMOS is currently the dominant technology in digital VLSI. Two components contribute to the power dissipation in CMOS circuits. The static dissipation is due to leakage current, while dynamic power dissipation is due to

switching transient current as well as charging and discharging of load capacitances [7]. Since the amount of leakage current is usually small, the major source of power dissipation in CMOS circuits is the dynamic power dissipation.

Dynamic power dissipation appears only when a CMOS gate switches from one stable state to another. Thus, the power consumption can be reduced if one can reduce the switching activity of a given logic circuit without changing its function. [2]

The power dissipation in CMOS circuits [7] is given by,

$P = (1/2)*C*V^2*f*N,$

Where,

P is the power dissipation,

C is the load capacitance,

V is the supply voltage,

f is the frequency of the clock,

N is the total number of switching activities in one clock cycle.

Dynamic power is due to the switching activities. So, by reducing the switching activity the dynamic power can be reduced.

1.2) Braun array multiplier

It is a simple parallel array multiplier generally called as carry save array multiplier. It has been restricted to perform signed bits. The structure consists of array of AND gates and adders arranged in the iterative manner and no need of logic registers. Array multiplier has regular structure. Since it is regular, it is easy to layout.

1.2.1) Architecture

An n*n bit Braun multiplier is constructed with n (n-1) adders and n2 AND gates.

As shown in figure 1.1 where,

X: 4 bit input

Y: 4 bit input

P: 8 bit output

Pn = Xi*Yi

The internal structure of the full adder can be realized using FPGA. Each products can be generated in parallel with the AND gates. Each partial product can be added with the sum of partial product which has previously produced by using the row of adders. The carry out will be shifted one bit to the left or right and then it will be added to the sum which is generated by the first adder and the newly generated partial product [2].

1.2.2) Advantages

1. It has a regular structure. Since it is regular, it is easy to layout.
2. Its ease of design for a pipelined architecture.

1.2.3) Disadvantages

1. It cannot stop the switching activity if the bit coefficient is zero that ultimately results in unnecessary power dissipation.
2. Size, as operand sizes increase, arrays grow in size at a rate equal to the square of the operand size.

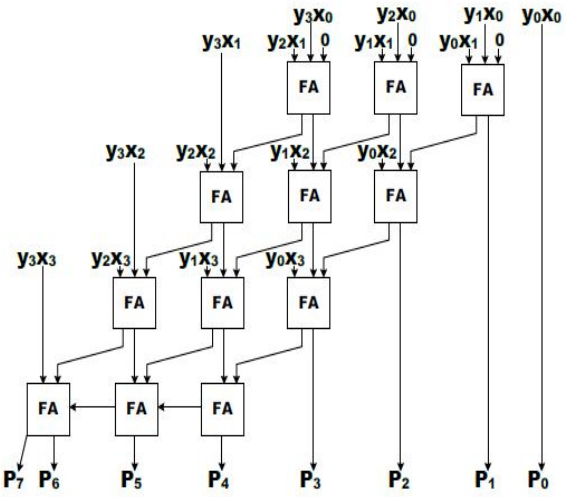

Fig 1.1Braun array multiplier

BYPASSING TECHNIQUES

2.1) Column bypassing technique

2.1.1) Architecture

The Column parallel multiplier operates by computing the partial products in parallel and by shifting and accumulating the partial products. Switching activity is poorly correlated with the input coefficient. In particular, reducing the switching activity of the component used in the design can minimize the power dissipation. It consists of three state gates, full adder and multiplexers. The inputs i.e. the partial products to be summed up are given to the full adder

through three state gates [4]. The enable input to the three state gates and multiplexers is the corresponding multiplier bit [7].figure 2.1 shows the multiplier of column bypassing technique.

2.1.2) Advantages

1. This technique reduces the switching.

2.1.3) Disadvantages

1. Number of columns switched depends on the number of ones in the multiplicand.
2. Less switching activity of the components can be achieved if the multiplicand contains more zeros than ones.

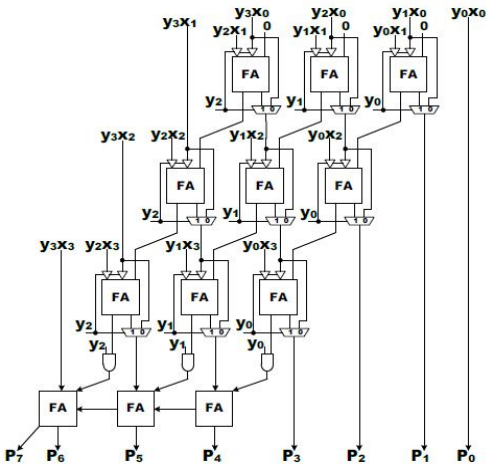

Fig 2.1 Column bypassing techniques

2.2) Row bypassing technique

2.2.1) Architecture

The Row bypassing multiplier reduces the switching activity by bypassing the row in which the multiplier bit is zero. That means in the multiplier if a bit is zero then that row of adders will get disabled. Here a special circuitry called adding cell is used instead of full adders.

It consists of three state gates, full adder and multiplexers. The inputs i.e. the partial products to be summed up are given to the full adder through three state gates. The enable input to the three state gates and multiplexers is the corresponding multiplier bit. If this bit is zero then the

three state gates goes into high impedance state [7] and thus inputs are not given to the full adder. The previous sum is only taken as the present sum.

If this bit is one then the three state gates gets enabled and the inputs are given to the full adder. Thus the sum is generated and this is taken as the present sum. In this way the switching activity can be reduced if the multiplicand bit is zero. figure 2.2 shows the multiplier of row bypassing technique.

2.2.2) Advantages

1. If multiplier bit is zero then that row of adders will get disabled.

2.2.3) Disadvantages

2. It needs extra correcting circuitry.

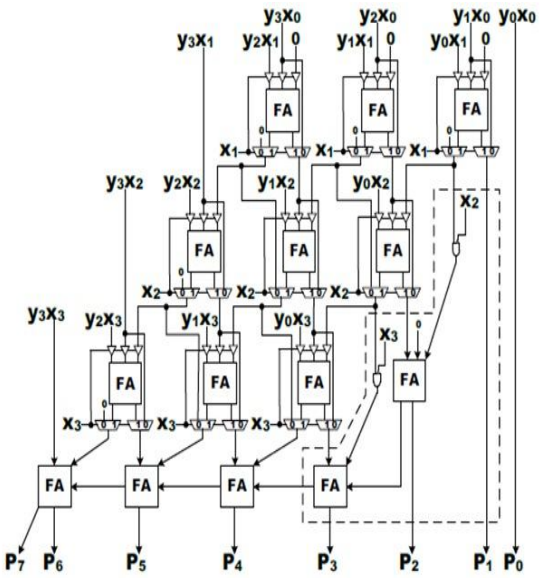

Fig 2.2 Row bypassing techniques

2.3) Row and Column bypassing technique

2.3.1) Architecture

Based on the operation simplification of full adders in an array multiplier, a low-power multiplier with row and column bypassing can be obtained. each simplified adder, A+1, in the CSA array is only attached by one tri-state buffer and two 2-to-1 multiplexers and each

simplified adder A+B+1, in the CSA array is only attached by two tri-state buffers and two 2-to-1 multiplexers.[1] figure 2.3 shows the multiplier of row column bypassing technique.

2.3.2) Advantages

1. Different modified adder cells are used.

2.3.3) Disadvantages

1. More circuitry hence requires more area.

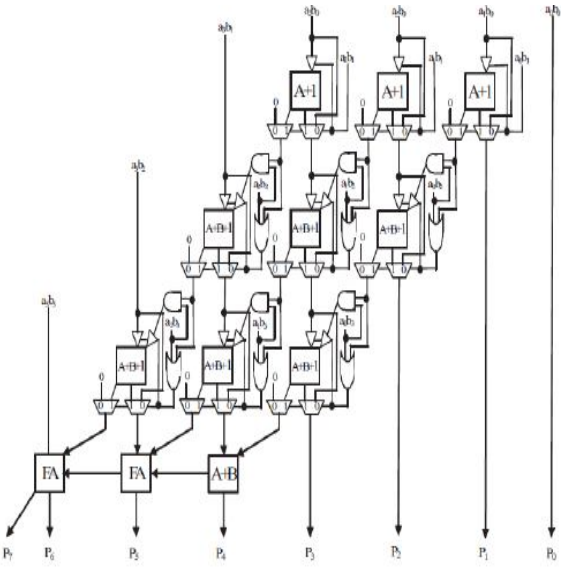

Fig 2.3 Row and column bypassing techniques

RESULTS AND DISCUSSION

The multiplier designs are simulated using ModelSim simulator. Simulation results for column bypassing, row bypassing, row and column bypassing as follow

3.1) Column bypassing technique

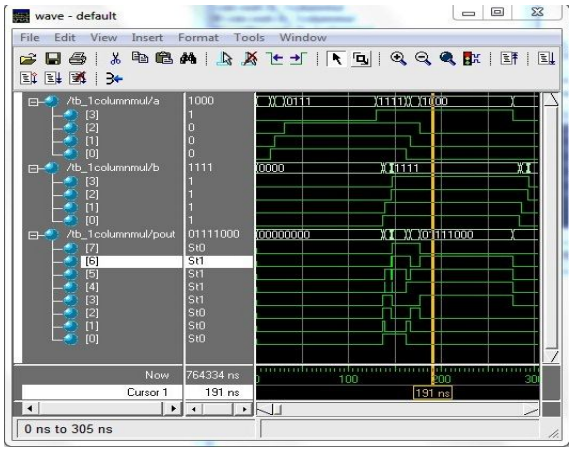

Fig 3.1 simulation result of column bypassing techniques

Description-

a=4bit input (1000)

b=4bit input (1111)

Pout =8bit output (01111000)

3.2) Row bypassing technique

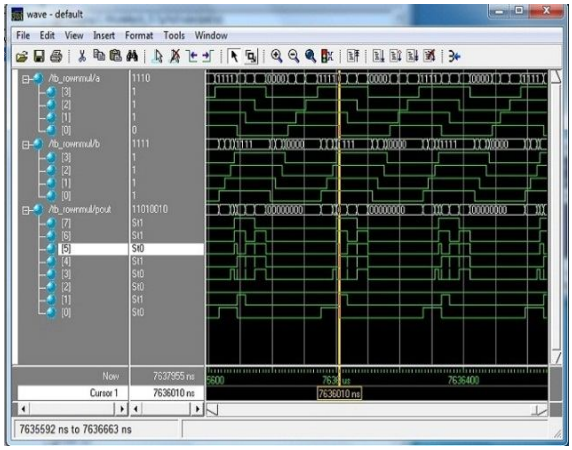

Fig 3.2 simulation result of Row bypassing techniques

Description

a=4bit input (1110)

b=4bit input (1111)

Pout =8bit output (11010010)

3.3) Row and Column bypassing technique

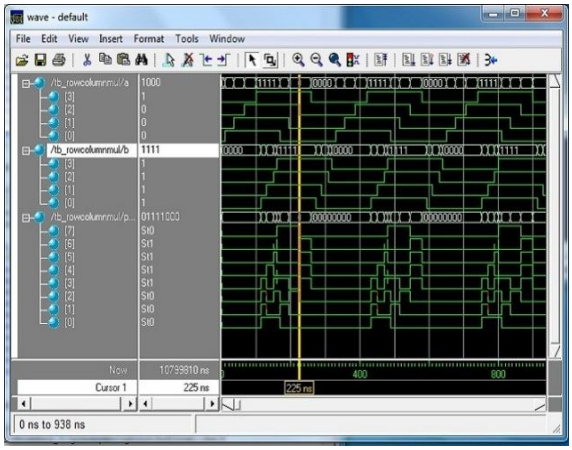

Fig 3.3 simulation result of Row and column bypassing techniques

Description-

a=4bit input (1000)

b=4bit input (1111)

Pout =8bit output (01111000)

This paper gives the design approaches about low power multipliers designs which reduce the power consumption. All the code is written in Verilog HDL language and the multipliers designs simulated in Modelsim simulator successfully.

It can be seen that theoretically this designs reduces switching Because of bypassing when some multiplier or multiplicand bits are zero and hence ultimately reduces power consumption of the multiplier.

Further work:

These designs are implementing on FPGA and finding path delay, cell area and power on Xilinx FPGA.

last stage of design uses ripple carry adder and hence delay increases. One way could be to use by replacing the ripple carry adder with fast adders (carry look ahead adder) in last stage of design is better.

REFERENCES

1. Anitha R, Bagyaveereswaran V ,"Braun Multiplier Implementation using FPGA with Bypassing Techniques", International Journal of VLSI design & Communication Systems (VLSICS) Vol.2, No.3, September 2011.

2. M. C. Wen, S. J. Wang and Y. M. Lin," Low power parallel multiplier with column bypassing" IEEE International Symposium on Circuits and Systems, pp.1638-1641, 2005.

3. J. sudha rani, R. N. S. Kalpana," Design of low power column bypass multiplier using fpga" International Journal Of Computational Engineering Research (ijcer) Vol. 3 Issue. 2, feb2013

4. "optimized multiplier using bypass technique" by Prof. P. P. Rane and Usha G. Chavan The International Journal of Computer Science Applications(TIJCSA)volume1,n0.2, April 2012.

5. Dr. Chirag Sharma Laxman s, Darshan Prabhu R, Mahesh shetty, Manjula BM, "FPGA Implementation of Different Multiplier Architectures" IJETAE june 2012 Vol II,issue6.

6. Samir Palnitkar, Verilog HDL-A guide to Digital Design and Synthesis (SunSoft Press.)

7. Neil H. E. Weste, David Harris and Ayan Banerjee ,CMOS VLSI Design (pearson education Asia, third edition, 2006.

8. C. Krishnamacharya ,Ch. Sravanthi, K. Avinash, K. V. Uma "Design of low power 2-D multiplier using Bypassing Techniques" IJIRS may 2013 Vol II.

9. "Braun Multipliers: A Delay Study" by Mohammed H. Al Mijalli Proceedings of the World Congress on Engineering 2012 Vol II WCE 2012, July 4 - 6, 2012, London, U.K.

10. Priya stalin, p saravana kumar, k saravanan, s sharu, tanmay talukdar "An efficient architecture with bypassing techniques and pipelining" International Journal of Engineering Sciences Research-IJESR, Vol 04, Issue 02; March-April 2013.

11. Ms. Madhu Thakur ,Prof. Javed Ashraf "Design of Braun Multiplier with Kogge Stone Adder & It's Implementation on FPGA" International Journal of Scientific & Engineering Research, Volume 3, Issue 10, October-2012.