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A PATH FOR HORIZING YOUR INNOVATIVE WORK

PREAMPLIFIER STAGE OF LVDS RECEIVER

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Abstract: Ever increasing demands of The processing speeds require very high speed and power efficient interconnections between the ICs. Such connections are governed by various standards, LVDS is one among them. In order to meet the requirements of high speed, low noise communication between ICs, the Low Voltage Differential signalling (LVDS) protocol is used. This paper studies the design of preamplifier stage of LVDS receiver. Due to the differential transmission technique and the low voltage swing, LVDS allows high transmission speeds and low power consumption at the same time.

Keywords: LVDS, differential amplifier, CS amplifier

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INTRODUCTION

Board level chip interfaces are demanding very high speed, power efficient interfaces. The ever increasing processing speed of microprocessor motherboards, optical transmission links, intelligent hubs and routers, etc..., pushing the off-chip data rate into the gigabits-per second range. However, unlike internal clocks, chip-to-board signaling gains little benefit in terms of operating frequency from the increased silicon integration. In the last decade, high data rates were achieved by massive parallelism, with the disadvantages of increased complexity and cost for the IC package and the printed circuit board (PCB). For this reason, the off-chip data rate is expected to move to the range of Gb/s-per-pin in the near future.[2] [3]

While the reduction of the power consumption is of great concern in battery-powered portable systems, it is also required in other systems to reduce the costs related to packaging and additional cooling systems. Some of today's biggest challenges that remain to be solved include: the ability to transfer data at fastest rate possible, low power systems than currently available and economical solutions to overcome the physical layer bottleneck.

Data transmission standards like RS-422, RS-485, SCSI and others have their own limitations notably in transferring raw data across a medium. Optical fibers are also costly and area inefficient for long distances. Thus, low-cost, high-speed parallel links and serial links using copper cables are an attractive solution for such applications. In this regard, Low-voltage Differential Signaling (LVDS) technology was developed in order to provide a low-power and low-voltage alternative, to other high-speed I/O interfaces for point-to point transmission.[4][5]

1.1) Preamplifier

This stage of the LVDS receiver is to reject the common mode noise. Hence, too much of amplification is not necessary, but a very good bandwidth is required. Therefore, a very good differential amplifier along with ESD protection circuit is used to welcome the incoming signal at the receiver side.

The amplifier stage is responsible for accommodating a very wide range of common mode signal; this is because the signal travelling long distances (from transmitter to receiver) will be affected by the external noise. Also, the ground level can shift to a different value. The output signal of the Pre-Amplifier stage has to be a differential signal which is riding on a constant DC signal, in order to bias the next stage of the receiver circuit.

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FOLDED CASCODE DIFFERENTIAL AMPLIFIER

2.1) Architecture

Folded Cascode has a special kind of arrangement in terms of the flow of current in the amplifier circuit. The CS amplifier (M1 and M2) acts as the voltage to current converter in the circuit, here the CS amplifier has the source degeneration resistor, i.e. the current source M3, gate to drain resistance(rds2). The converted current is folded and pushed into the CG amplifier (M6 and M7) whose load is the series combination of resistance (R1 and R2) and the MOS diode (M8 and M9).The amplified current following through the MOS diode and the resistance load produce the output voltage with the load capacitor (CL). The figure 4.1 gives the folded cascode differential amplifier which is used in this project. The MOS diode is used as the load. The diode along with the resistance will provide less resistive load, but the bandwidth is improved, along with this, the drop across the resistance, which means less variation of voltage across the resistance if there is variation of resistance.

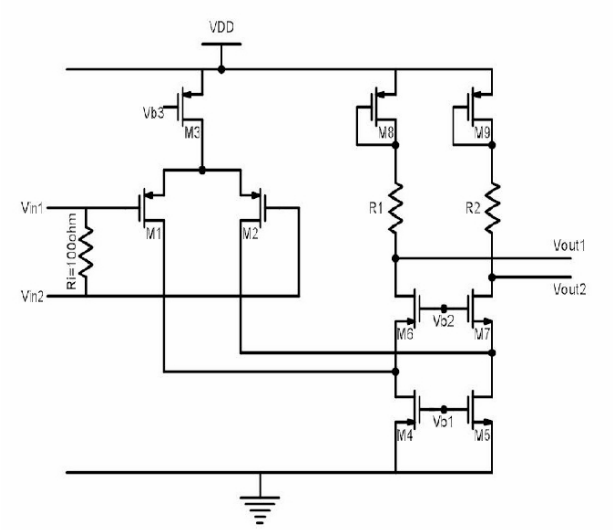

Fig 2.1 Folded Cascode Differential Amplifier circuit

2.2) Electrical Specification for Preamplifier

All the specifications of the system are derived in accordance with the IEEE 1596.3 - 1996 Std.[1]

Input common mode voltage =50mV to 2.35 V.

Input differential voltage=-100mV to +100mV.

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Output common mode voltage=1.65V.

Output differential voltage=+300mV to -300 mV.

load capacitor=20fF.

Slew rate=2V/nsec.

S=I3/Cl

PMOS design The current owing in pmos transistor

I3=S*Cl

I3=(2V/nsec)*(20fF)

I3=40uA

I2 or I1=I3/2

I2 or I1=40uA/2

I2 or I1=20uA

Take Vin1=Vin2=50mV to 2.35V.

Rin=100ohm

Take Vgs=Vb1

current owing in PMOS

I4 and I5=1.5*I1

I4 and I5 = 1.5*40uA

I4 and I5 =60uA

I4=I5=30uA

I1+I2=I3+I4

I1+I2-I3-I4=0

I6 and I7= (I4 or (I5)-I1)

-

I6 and I7=(60uA-20uA)

I6 and I7=40uA

Vout1 and Vout2=3.3/2=1.65V

Take V less then Vout

so V=.04V

Rin=.04/40uA

Rin=1Kohm

We need to calculate M8 and M9

so, V8 and V9=(Vout-Vrl)

V8 and V9=1.65-.08

V8 and V9=1.57V

Vgs and Vds=1.57V

PMOS design

To calculate the M8 and M9 W8/L8p values

I=[un*Cox*(W8/L8)p*Vgs-Vth2]

Vgs=1.57V

Vth=.7V

Cox=eox/tox

Cox=(3.9*8.854)/(2)

Cox=1.726 F/cm2

up=500cm2/Vsec

I6 and I7=40uA

For M8 and M9

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W8/L8p=[I6 /un*Cox*(Vgs-Vth)]

W8/L8p=40/(500*1.7261.57-.7)

W8/L8p=40/750.81

W8/L8p=50um

NMOS design

M4 and M5

Vb1=2V

I4 and I5=60uA

I4=[un*Cox*(W4/L4)n*Vgs-Vth2]

60uA=[637.51*1.726*(W4/L4)n*(2-.7)2]

(W4/L4)n=60uA/637.51*1.726*1.69

(W4/L4)n=40um For nmos transistors M6 and M7

Take un=3.142cm/Vsec

I6=[un*Cox*(W6/L6)n*(Vgs-Vth)2]

40=[3.142*1.172*(W6/L6)*(1.8-.7)2]

(W6/L6)n=[40/(3.142*1.172*1.1)]

(W6/L6)=20um

take up=1.142cm2/Vsec For pmos transistor M3 I3=[un*Cox*(W3/L3)p*(Vgs-

Vth)2]

40u=[1.142*1.172*(W3/L3)p*(.49)]

(W3/L3)p=40u/[1.142*1.172*.49]

(W3/L3)p=60um For pmos transistors M1 and M2

I1=[up*Cox*(W1/L1)p*(Vgs-Vth)2]

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I1=[1.142*1.172*(W1/L1)p*(2.4-.7)2]

(W1/L1)p=[30uA/(1.141*1.172*1.7)]

(W1/L1)p= 20um

2.3) Design Steps

The design steps of the folded cascode differential amplifier are as given below.

Slew Rate-The slew rate required at the output determines the tail current of the differential pair. Therefore ITail = 400uA.

Bias current in Cascode Pair-The bias current following in the cascode pair (M6 and M7) will be nearly equal to the tail current. This defines the W/L ratio of the cascode devices.

Maximum current in the arm-The current from the differential pair and the current from the cascode device together is to be accommodated by the n-MOS, M5 and M6. Hence this defines the W/L ratio of the M5 and M6.

Maximum input common mode voltage range-The maximum input common mode voltage range defines the minimum over-drive voltage that is required to keep the p-MOS M3, hence the W/L of M3 will be defined by the same.

Minimum input common mode voltage range-The minimum input common mode voltage defines the maximum overdrive voltage of the n-MOS M5 and M6, which defines W/L of MOSFETs M5 and M6.

Output Common mode voltage-The output common mode voltage is VDD. VMOS-Diode VResistor-The voltage drop across the diode is fixed by a constant W/L of MOS. The current owing through the resistor will define the voltage across the resistor. Hence, the resistor value is fixed by the voltage drop required to meet the output common mode specification.

Input resistance-The resistance of 100 is put as the terminating resistance of the LVDS receiver in order to match with the impedance of the transmission line which is 100 as per the IEEE Std 1596.3.[1].

2.4) Bias circuit of the Folded Cascode Differential Amplifier

The Folded Cascode desires a special type of bias network, in order to keep all the MOSFETs in saturation region. The Bias network uses a current reference. The current reference used is

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same as the reference used in any IC where this receiver fits in. The bias network designed for the Folded Cascode Differential Amplifier is as given in figure 4.2.

The different voltages required by the Amplifier circuit like Vb1, Vb2 and Vb3 are generated by the MOSFETs used as diodes. The maximum current in the arm defines the value of Vb1, which is generated by the n-MOS diode M17. The bias point of the CG amplifier of the circuit is Vb2 and it is derived from the n-MOS M18.The M18 is a slightly long channel MOS compared to M17, in order to keep the gate of M6 and

M7, slightly higher than M5 and M6, Yet all the 4 MOSFETs are to be in saturation, which can be achieved by the reduction in VDSsat of the MOSFETs. The M3 of the amplifier is biased with the gate voltage Vb3 generated from the MOS M10.This M10 is a very wide MOSFET since the VDSsat of M3 should be very less to accommodate the large common mode variation at the input of the differential amplifier pair.

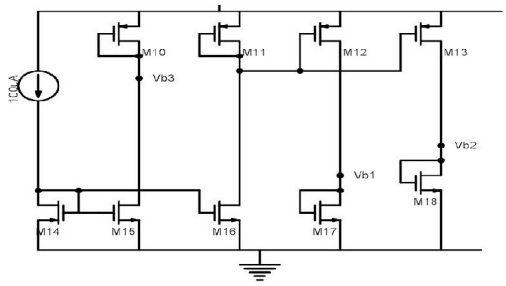

Fig 2.2 Bias circuit

RESULTS AND DISCUSSION

The schematic design and layout design are carried out using CADENCE tool for 0.18µm technology (UMC180nm)

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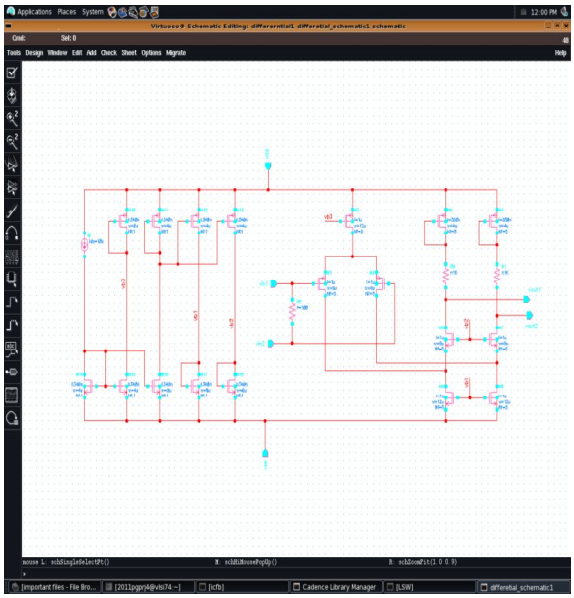

Fig 3.1 The Differential Amplifier Schematic

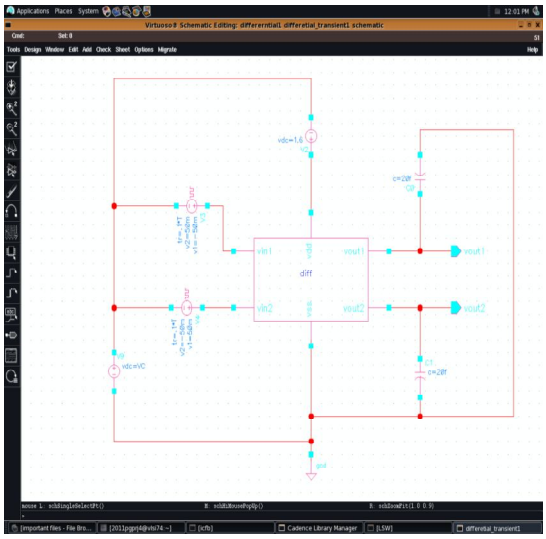

Fig 3.2 The differential transient Schematic

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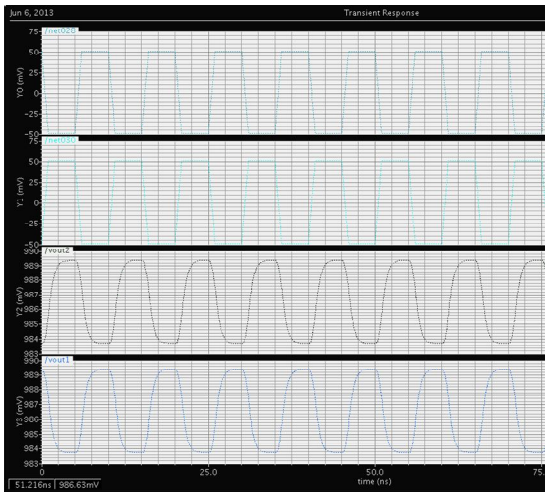

Fig 3.3 The differential transient response output

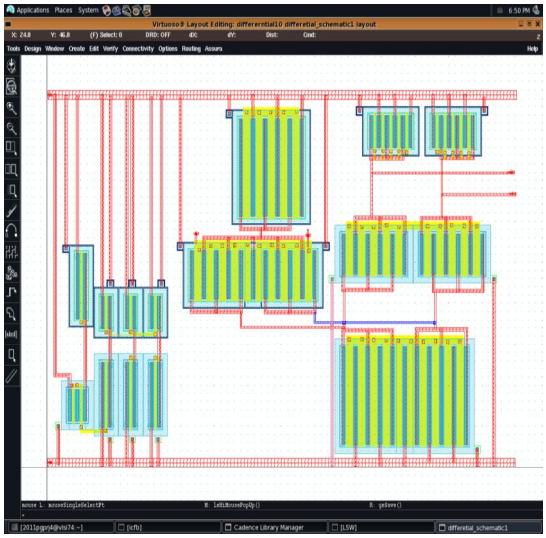

Fig 3.4 layout of the Differential amplifier

CONCLUSION:

In this paper we designed a preamplifier stage of LVDS receiver at 0.18um technology.

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