INTERNATIONAL JOURNAL OF PURE AND APPLIED RESEARCH IN ENGINEERING AND TECHNOLOGY

A PATH FOR HORIZING YOUR INNOVATIVE WORK

A LITERATURE REVIEW ON A LOW-POWER SINGLE-PHASE CLOCK MULTIBAND FLEXIBLE DIVIDER

DEVENDRA O. RAPELLI[1], DIVYA MESHRAM[2], MOHINI VYAWHARE[3]

1. M-Tech, Department Of Electronics Engineering, PCE, Nagpur.
2. Associate Prof., Department Of Electronics Engineering, PCE, Nagpur.
3. Assistant Prof., Department Of Electronics Engineering, PCE, Nagpur.

Accepted Date: 05/03/2015; Published Date: 01/05/2015

Abstract: With higher level of integration the demand for lower cost, lower power, and multiband RF circuits increased in conjunction to the need. In this proposed system a low-power single-phase clock multiband flexible divider for Bluetooth, Zigbee, IEEE 802.15.4 and 802.11 a/b/g WLAN frequency synthesizers is proposed based on pulse-swallow topology and is implemented using a 0.18- m CMOS technology. The multiband divider consists of a proposed wideband multi modulus 32/33/47/48 pre scaler and an improved bit-cell for swallow (S) counter and can divide the frequencies in the three bands of 2.4–2.484 GHz, 5.15– 5.35GHz, and 5.725–5.825 GHz with a resolution selectable from 1 to 25 MHz. and consumes power of 0.96 and 2.2 mW in 2.4- and 5-GHz bands, respectively, when operated at 1.8-V power supply.

Keywords: DFF, E-TSPC, Frequency Synthesizer, High-Speed Digital Circuits, True Single-Phase Clock (TSPC). Wireless LAN (WLAN).

Corresponding Author: MR. DEVENDRA O. RAPELLI

PAPER-QR CODE

Access Online On:

www.ijpret.com

How to Cite This Article:

Devendra O. Rapeli, IJPRET, 2015; Volume 3 (9): 196-202

INTRODUCTION

For mobile wireless communications, low-power operations are of crucial importance for the mobile units as the battery lifetime is limited by the power consumption and the low power consumption also helps to reduce the operating temperature resulting in more stable performance. For the modern transceiver architecture, a fully integrated frequency synthesizer with low power voltage-controlled oscillators (VCO) for quadrature signal generation and low power frequency dividers with multi-channel selection is always a topic of interest in research.

Phase-locked loops (PLLs) are widely used in radio frequency synthesis. The PLL based frequency synthesizer is one of the key building blocks of an RF front-end transceiver. The PLL frequency synthesizer system is mainly designed to ensure the accuracy of its output frequency under operating conditions. In the previous design [1], a dynamic logic multiband flexible integer-N divider based on pulse-swallow topology is proposed which uses a low-power wideband 2/3 prescaler [4] and a wideband multimodulus32/33/47/48.

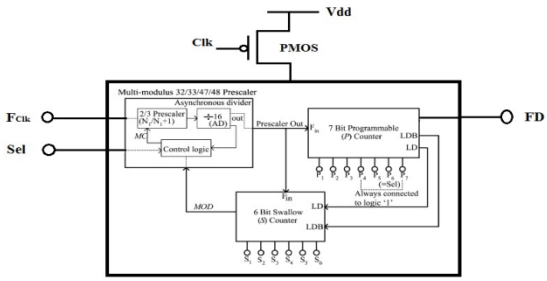

Figure.1.Proposed dynamic logic multiband flexible divider using SleepyP transistor

In this paper a new method for designing a dynamic logic multiband flexible integer-N-divider has been proposed which is developed using a sleep transistor based and wideband multimodulus 32/33/47/48 prescaler with low-power wideband 2/3 prescaler and an integrated S counter as shown in Fig. 1. A sleep transistor is referred to either a PMOS or NMOS high Vth transistor that connects permanent power supply to circuit power supply which is commonly called “virtual power supply”. The sleep transistor is controlled by a power management unit to switch on and off power supply to the circuit.

II DESIGN CONSIDERATIONS

In the case of high-speed digital circuits propagation delay and power consumption are the important parameters. The maximum operating frequency of a digital circuit is given by,

$$F_{max} = \frac{1}{tpLH + tpHL} \quad (1)$$

The tpLH and tpHL denote the propagation delays of the low- to-high and high-to-low transitions of the gates, respectively. In CMOS digital circuits total power consumption is determined by the switching and short circuit power. The switching power is linearly proportional to the operating frequency and is given by the sum of switching power at each output node as in

$$P_{switching} = \sum_{i=1}^{n} F_{clk} C_{li} V_{dd}^2 \quad (2)$$

Where n is the number of switching nodes, fclk is the clock frequency, CLi is the load capacitance at the output node of the ith stage, and Vdd is the supply voltage. Normally, the short-circuit power occurs in dynamic circuits when there exists direct paths from the supply to ground which is given by $P_{sc} = I_{sc} * V_{dd}$ **(3)**

Where Isc is the short-circuit current. The short-circuit power is much higher in E-TSPC logic circuits than in TSPC logic circuits. However, TSPC logic circuits exhibit higher switching power compared to that of E-TSPC logic circuits due to high load capacitance. For the E-TSPC logic circuit, the short-circuit power is the major problem. The E-TSPC circuit has the merit of higher operating frequency than that of the TSPC circuit due to the reduction in load capacitance, but it consumes significantly more power than the TSPC circuit does for a given transistor size. The following analysis is based on the latest design using the popular and low-cost 0.18-µmCMOS process.

A). Sleep Transistor Approach the most well-known traditional approach is the sleep approach [3]. In the sleep approach, both (i) an additional "sleep" PMOS transistor is placed between VDD and the pull-up network of a circuit and (ii) an additional "sleep" NMOS transistor is placed between the pull-down network and GND. These sleep transistors turn off the circuit by cutting off the power rails. By cutting off the power source, this technique can reduce leakage power effectively. However, the technique results in destruction of state plus a floating output voltage.

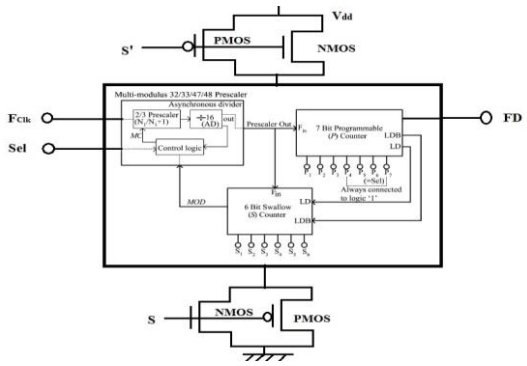

Figure.2.Proposed dynamic logic multiband flexible divider using sleep transistor

B). Dual Stack Approach In dual stack approach [7], 2 PMOS in the pull- down network and 2 NMOS in the pull-up network are used. The advantage is that NMOS degrades the high logic level while PMOS degrades the low logic level. Compared to previous approaches it requires greater area. The delay is also increased.

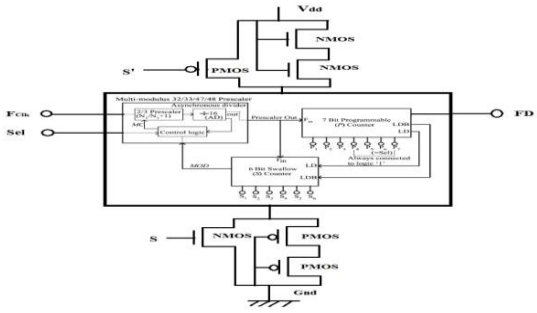

Figure.3.Proposed dynamic logic multiband flexible divider using dual stack

III MULTIMODULUS 32/33/47/48 PRESCALAR

The proposed wideband multimodulus prescaler is similar to the 32/33 prescaler but with an additional inverter and a multiplexer. The proposed prescaler can divide the input frequency by 32, 33, 47, and 48 is shown in Fig. 6. It performs additional divisions (divide-by-47 and divide-by-48) without any extra flip-flop, thus saving a considerable amount of power and also reducing the complexity of multiband divider. The multimodulus prescaler consists of the wideband 2/3 **(N1 / (N1 + 1))** prescaler, four asynchronous TSPC divide-by-2 circuits **((AD) = 16)** and combinational logic circuits to achieve multiple division ratios. Besides the usual **MOD** signal for controlling **N / (N + 1)** divisions, the additional control signal Sel is used to switch the prescaler between 32/33 and 47/48 modes.

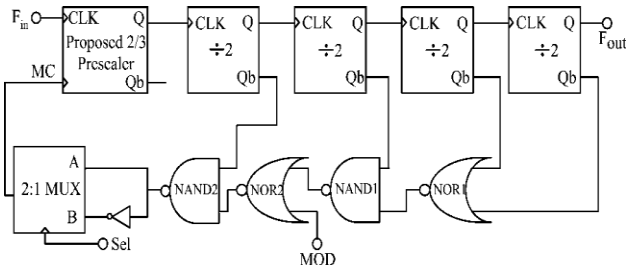

Figure4 Multimodulus32/33/47/48Prescaler.

IV MULTIBAND FLEXIBLE DIVIDER USING SLEEP TRANSISTORS

The single phase clock multiband flexible divider using sleep transistor which is shown in Fig. 1 consists of the multimodulus 32/33/47/48 prescaler, a 7-bit programmable -counter and a 6-bit swallow counter. The multi- modulus 32/33/47/48 prescaler is briefly discussed in Section IV. The control signal decides whether the divider is operating in lower frequency band (2.4 GHz) or higher band (5–5.825 GHz).

A. Swallow S-counter

The 6-bit -counter shown in Fig. 5 consists of six asynchronous loadable bit-cells, a NOR-embedded DFF and additional logic gates to allow it to be programmable from 0 to 31 for low-frequency band and from 0 to 47 for the high-frequency band. The asynchronous bit-cell used in this design uses two additional transistors M6 and M7 whose inputs are controlled by the logic signal **MOD**. If **MOD** is logically high, nodes S1 and S2 switch to logic“0” and the bit-cell doesn’t perform any function. The **MOD** signal goes logically high only when the S-counter finishes counting down to zero. If **MOD** and **LD** are logically low, the bit-cell acts as a divide-by-2 unit. If **MOD** is logically low and **LD** is logically high the input bit **PI** transferred to the output..

B. Programmable P-counter

The programmable P-counter used in the design of the fully programmable divider is a 7-bit asynchronous down counter. The P-counter is designed with 7 reloadable TSPC D flip-flops (DFF) and an end-of- count (EOC) detector which has reload circuit in it. Since the counter is asynchronous and based on the ring topology, the complementary output of the first DFF is fed as clock to the input of next flip-flop. In the initial state, all the reloadable FF’s are loaded by the

programmable pins **P1-P7**. As the counter is triggered by the output of the prescaler, the **P**-counter starts down counting till the state "0000000" is reached. Once this state is detected by the EOC logic circuit, the load (**LD**) signal goes high to reset all loadable FF's to the initial state. The 32/33 prescaler scales the input 2.4 GHz signal by a value of 32 or 33 such that the **P** and **S** counters will be working in the frequency range of 72 - 78 MHz in order to obtain the 1 MHz frequency output.

V RESULTS AND DISCUSSION

Comparison between previous work and present work we can reduce the power consumption and reduce the 7 number of stages

Table.1,.PERFOMANCE OF DIFFERENT DIVIDERS

Reference	Sleepy N	Sleepy approach	Dual stack
Process(µm)	0.18	0.18	0.18
Supply volt(v)	3.3	3.3	3.3
Power (mW)	1.32e-03	2.19e-03	2.73e-03

VI CONCLUSIONS

In this paper a lower-power single-phase clock multiband flexible divider with sleep transistor, the circuit simplicity leads to reduced power consumption, reduced number of gates required and hence a reduced area requirement we have implemented fully programmable multi-band flexible divider for Bluetooth, Zigbee, IEEE 802.15.4 and 802.11 a/b/g frequency synthesizers. However, implementing frequency synthesizer which covers 2.4 GHz ISM band and 5-6 GHz WLAN using multi-band divider is very challenging as it requires low power, low phase noise dual-band VCO. When compared to previous power consumption 56.74% has been reduced. In future, more work has to be done in exploring better ways of implementing the low power techniques

VII ACKNOWLEDGMENT

The author would like to thank prof. Divya Meshram and prof. M. Vyawhare for their valuable discussion and suggestions.

VIII REFERENCES

1. Vamshi Krishna Manthena, Manh Anh Do, Chirn Chye Boon, and Kiat Seng Yeo., "A Low-Power Single-Phase Clock Multiband Flexi- ble Divider" , IEEE Trans. Very Large Scale Integr, (VLSI) Syst., vol. 20, no. 2, Feb. 2012

2. Yin-Tsung Hwang and Jin-Fa Lin., "Low Voltage and Low Power Divide-By-2/3 Counter Design Using Pass Transistor Logic Circuit Technique", IEEE Trans. Very Large Scale Integr.(VLSI) Syst., vol. 20, no. 9, Sep. 2012

3. S. Mutoh et al., "1-V Power Supply High-speed Digital Circuit Technology with Multithreshold-Voltage CMOS," IEEE Journal of Solis-State Circuits, Vol. 30, No. 8, pp. 847-854, August 1995.

4. S. Pellerano et al., "A 13.5-mW 5 GHz frequency synthesizer with dynamic-logic frequency divider," IEEE J. Solid-State Circuits, vol. 39, no. 2, pp. 378–383, Feb. 2004.

5. S. Vikas et al., "1 V 7-mW dual-band fast-locked frequency synthesizer," in Proc. 15th ACM Symp. VLSI, 2005, pp. 431–435.