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DESIGN AND IMPLEMENTATION OF TRUNCATED MULTIPLIER FOR DSP APPLICATIONS

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Abstract: Truncated multiplier is required in digital signal processor operations such as filtering, convolution, and fast Fourier or discrete cosine transform. These operations can be done using standard parallel multiplier which needs more computation as compared to truncated multiplier. Multiplication is one of the most area consuming arithmetic operations in high-performance circuits. In most signal processing applications, a rounded product is desired to avoid large area. Truncated multipliers having significant improvements in area, delay and power requirement. The proposed method finally reduces the number of full adders and half adders during the reduction of level. By this proposed method, area can be saved up to large extent. Finally the LSB part is compressed by using operations such as delete non require bits, reduce the level, truncation, round up result using correction logic and final addition which offers precision improvement.

Keywords: Deletion, reduction, truncation, rounding, final addition, truncated multiplier.

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INTRODUCTION

The multiplier is an essential element of digital signal processing operations such as filtering and convolution. Most of the digital signal processing operations such as Discrete Cosine Transform (DCT) or Discrete Wavelet Transform (DWT) is accomplished by repetitive multiplication and addition. Hence the speed of these operations exclusively depends upon the speed of the multiplication operation being performed. It has been observed that the multiplier requires the longest delay among the basic operational blocks in a system; hence the critical path is predominantly determined by the multiplier. Also, the standard multiplier has been observed to consume comparatively more area and power. Therefore a design which will reduce the consumed area or power or speed or any combination of the above three parameters is of research interest.

There is need of standard multiplier for DSP application such as filtering, convolution, and fast Fourier or discrete cosine transform. These operations for DSP application can be performed using truncated multiplier. Standard multiplier produces 2n bit output for n x n bit multiplication, whereas truncated multiplier gives n-bit output. This truncated multiplier follows steps such as delete non require bits, reduce the level, truncation, round up result using correction logic and final addition which offers precision improvement.

I. LITERATURE REVIEW

A faithfully rounded truncated multiplier design is presented where the maximum absolute error is guaranteed to be not more than 1 unit of least position. In the proposed method, they jointly considers the delete non require bits, reduce the level, truncation, round up result using correction logic and final addition of partial product bits in order to minimize the number of full adders and half adders during tree reduction.

In addition, the truncated multiplier design also has smaller delay due to the smaller bit width in the final carry-propagate adder. By using this method we can be easily extended to signed or Booth multiplier design[1].

Low-cost finite impulse response (FIR) designs are presented using the concept of faithfully rounded truncated multipliers.

They jointly consider the optimization of bit width and hardware resources without sacrificing the frequency response and output signal precision. Non uniform coefficient quantization with proper filter order is proposed to minimize total area cost. Multiple constant multiplications-

accumulations in a direct FIR Structure is implemented using an improved version of truncated multipliers[2].

II. REDUCTION SCHEMES OF PARALLEL MULTIPLIERS

PP (partial product) generation produces partial product bits from the multiplicand and multiplier. PP reduction is used to compress the partial product bits to two. Finally the partial products bits are added by using carry propagate addition. Two famous reduction methods are available,

1. Dadda tree

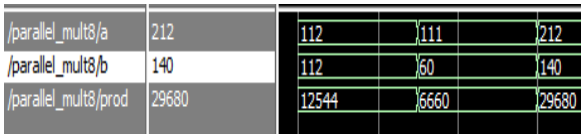
2. Wallace tree

Dadda reduction performs the compression operation whenever it required. Wallace tree reduction always compresses the partial product bits.

In this proposed work standard parallel multiplier is design & truncated multiplier design, introduces column-by-column reduction. The result is obtained from standard parallel multiplier and truncated multiplier gives close result. Truncated multiplier minimizes the half adders in each column because the full adder has high compression rate when compared to HA.

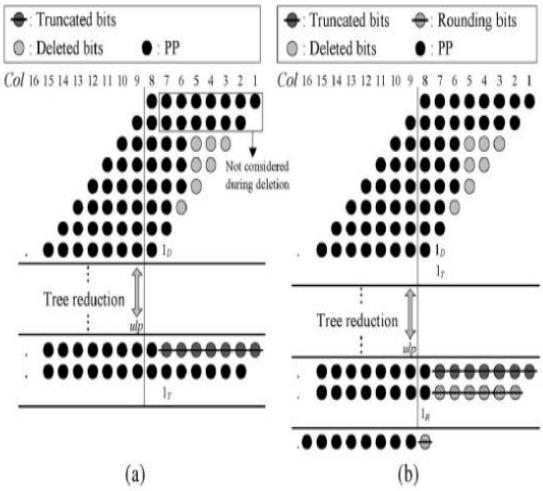
A parallel tree multiplier design usually consists of three major steps, i.e PP generation, PP reduction, and final carry propagate addition. PP generation produces PP bits from the multiplicand and the multiplier. The goal of PP reduction is to compress the number of PPs to two, which is to be added for final addition. Wallace tree reduction manages to compress the PPs as early as possible, whereas Dadda reduction only performs compression whenever.

In this proposed work we first design standard parallel 8x8 multiplier which gives following result.



This standard parallel 8x8 multiplier requires large number of component to design by virtue of its area requirement is more. Also it requires more power and propagation delay. To reduce this requirement of area, power and delay we proposed truncated multiplier.

III. PROPOSED TRUNCATED MULTIPLIER DESIGN



For convenience, we assume n×n unsigned multiplication of two numbers. The objective of a good multiplier is to provide a better result, high speed and low power consuming chip. To save area requirement and power consumption of a VLSI design. In a truncated multiplier, number of the least significant columns of bits in the partial product matrix are not formed. Fig1. Show 8x8 truncated multiplication. (a) Deletion, reduction and truncation. (b) Deletion, reduction, truncation, rounding with correction logic and final addition.

PROPOSED ALGORITHM

In proposed architecture we multiply 8x8 bits, and the bits are reduced in step by step manner. Deletion is the first operation performed in Stage 1 to remove the PP bits, as long as the magnitude of the total deletion error is no more than 2^{-P-1}. Then number of stages are reduce the final bit width without increasing the error. Fig. shows proposed truncated multiplier. This reduces the area and power consumption of the multiplier [3]. better result. For this we used Half Carry(HC), Full Carry(FC), Half Adder(HA), Full Adder(FA) logic to improve the result. Requirement of component for this truncated multiplier is less as compared to standard parallel multiplier; however it reduces the area required as well as delay and power. Following result is obtained for proposed 8x8 bit truncated multiplier which is approximately same as that of standard parallel multiplier with precision improvement.

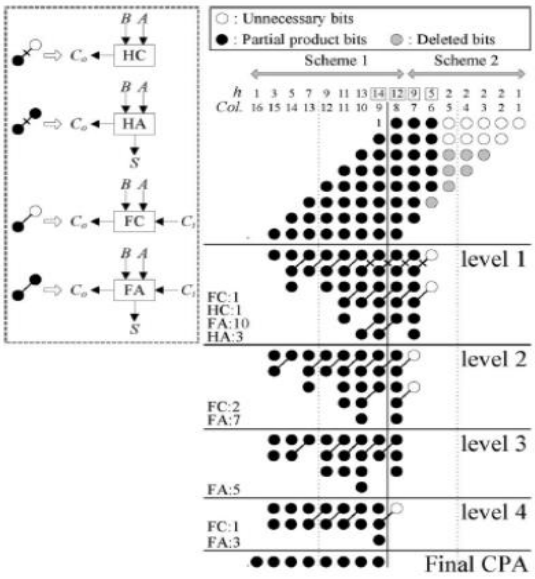
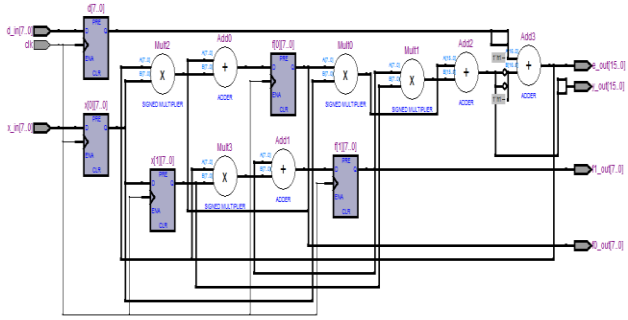


Fig. Proposed 8x8 bit truncated multiplier

IV. FUTURE POSSIBLE ENHANCEMENT

Truncated multiplier can be effectively implemented in FIR filter structure. Conventional FIR filer performs ordinary multiplication of co-efficient and input without considers the length. Thus the structure can be made effective by replacing the existing multiplier with the proposed fixed width truncated multiplier for visible area reduction.



V. SUMMARY OF RESULT

Parameter	Standard multiplier	Truncated multiplier
Total logic elements required	189	109
I/O thermal Power dissipation	33.67mW	33.61mW
Propagation delay	22.412 ns	19.366 ns
No of Component required	8 HA, 48 FA	3 HA, 32 FA,

1	HC, 4 FC

VI. CONCLUSION

We have presented a new truncated multiplier design by jointly considering the deletion, reduction, truncation, and final addition of PP bits. In this design we first observed result of standard parallel multiplier and then compare this result with truncated multiplier which is approximately same. Due to this implementation of truncated multiplier area reduces to large extent as compare to standard parallel multiplier.

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