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POINT PROCESSING OPERATION USING MIXED HDL PLATFORM FOR IMAGE PROCESSING

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Abstract: Application areas of signal processing have grown dramatically in importance in recent times, in parallel with the growth of powerful and low-cost processing chips. This has led, in turn, to many new applications, including multimedia delivery and hand-held communications delivery. Image is one of the most fundamental and significant features. The correctness and reliability of its results affect directly the comprehension machine system made for objective world. Image processing is one an important application among them, which has a strong mathematical basis. The implementation of Point processing algorithms on a field programmable gate array (FPGA) is having advantage of using large memory and embedded multipliers. The point processing techniques are using only the information in individual pixels to produce new images. This project focus on implementation issues of image enhancement algorithms like brightness control, contrast stretching, negative transformation, thresholding, filtering techniques on FPGA that have become a competitive alternative for high performance digital signal processing applications. XSG is a useful tool to understand fundamental Digital Signal Processing (DSP) algorithms for Field Programmable Gate Array (FPGA) implementation. FPGAs provide a better platform for real-time algorithms on application-specific hardware with substantially greater performance than programmable DSPs. By a brief analysis about display image and resource consumption after achieving on Spartan-6 development board, we can see the image using System Generator for FPGA algorithm design superiority, have the vast application prospects.

Keywords: Image Processing, Point Processing, Xilinx System Generator, FPGA

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INTRODUCTION

In today's modern computers, media information such as audio, images, and video have come to be necessary for daily business operations and entertainment. In this paper, we study digital images and its processing techniques, specifically point processing algorithms. Digital images are electronics snapshots taken of a scene or scanned from documents, such as photographs, manuscripts, printed texts, and artwork. The digital image is sampled and mapped as a grid of dots or picture elements (pixels). The digital image is picture information in digital form. The image can be filtered to remove noise and obtain enhancement [3]. It can also be transformed to extract features for pattern recognition. The image can be compressed for storage and retrieval, as well as transmitted via a computer network or a communication system. Digital image processing has found application in wide variety of fields of human endeavor. There is Number of well-defined processes which go to make up a typical image application. Acquisition, Enhancement, Restoration, Segmentation and Analysis are the steps needed by just about every application which involves image processing [4].

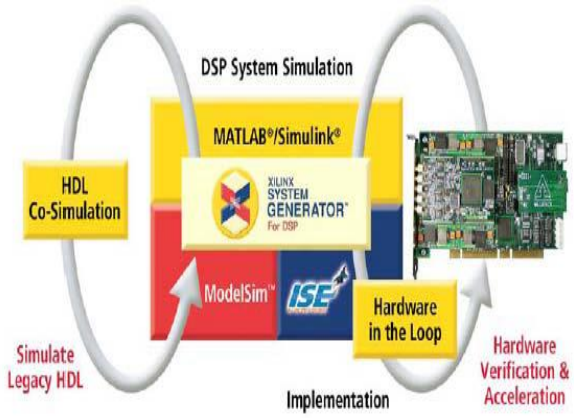
Once images are inside the computer system, or more specifically, once they are read inside a program, the images are nothing but matrices. Hence, all the operations that can be applied to matrices should theoretically be applicable to the images as well. Image arithmetic is the implementation of standard arithmetic operations, such as addition, subtraction, multiplication, and division for images. DSP functions are implemented on two primary platforms such as Digital Signal Processors (DSPs) and FPGAs [6]. FPGA is a form of highly configurable hardware while DSPs are specialized form of microprocessors. Most engineers prefer FPGA over DSP because Fast prototyping and turn-around time, Non-Recurring Engineering refers to the one-time cost of researching, developing, designing and testing a new product. Since FPGAs are reprogrammable, High-Speed & Low cost.

Digital image processing plays an essential role in the analysis and interpretation of remotely sensed data. Data obtained from Medical and Satellite Remote Sensing, which is in the digital form, can best be utilized with the help of digital image processing. The application domain of DSP over the past decade expanded because of the advance in VLSI technology. Application Specific Integrated Circuits (ASIC) and programmable DSP processors were the implementation choices for many DSP applications. But now, reconfigurable computing are being considered for system implementations because of the programmable of software and the functional efficiency of hardware. FPGAs are an attractive choice due to their low energy dissipation per unit computation, high performance, and reconfigurability. The parallel computing power of

the FPGA is extremely useful in the modern world of demanding applications like DSP, image and video processing etc.

System Generator [7] is a DSP design tool from Xilinx that enables the use of the Math works model-based design environment Simulink for FPGA design. It is a system level modeling tool in which designs are captured in the DSP friendly Simulink modeling environment using Xilinx specific Block set. All of the downstream FPGA implementation steps including synthesis and place and route are automatically performed to generate an FPGA programming file. System Generator provides many features such as System Resource Estimation to take full advantage of the FPGA resources, Hardware Co-Simulation [8] and accelerated simulation through hardware in the loop co-simulation; which give many orders of simulation performance increase [9,10,11]**.**

This system is implemented on FPGA board using a combination of MATLAB Simulink and Xilinx System Generator prototyping environment. The proposed implementation result is compared with conventional approach.



This techniques used for different applications depends on requirement and need. These techniques used in x-ray, digital mammography, CT scans, MRI, GOOGLE Maps etc.

LITERATURE REIEW

[1][R.Harinarayan,R.Pannerselvam,M.Mubarak Ali,Dhirendra Kumar Tripathi] In this paper FPGA-based architecture for edge detection algorithms has been proposed. FPGAs are providing a platform for processing real time algorithms on application-specific hardware with substantially higher performance than programmable digital signal processors (DSPs). The

proposed architecture can be used as a building block of a aerial imaging systems for navigation and for the pattern recognition.

[2] [A. Amaricai, O. Boncalo, M. Iordate, and B. Marinescu] In this paper authors proposed an accelerator for point process implemented on FPGA. The proposed architecture relies on a moving window consisting of 7x8 pixels, which performs the more computational complex operations of the algorithm. This project proposed an HW/SW code sign solution for point processing algorithm.

[3] [V. ELAMARAN, G.RAJKUMAR] In this paper, a real-time image processing algorithms are implemented on FPGA. Implementation of these algorithms on a FPGA is having advantage of using large memory and embedded multipliers. Advances in FPGA technology with the development of sophisticated and efficient tools for modeling, simulation and synthesis have made FPGA a highly useful platform

[4] [Sudeep,K..C.J. Majumdar] Introduced novel architecture for real time implementation of edge detectors on FPGA. Int J. Comput. Sci.8:193-202.In this paper FPGA based implementation of conventional edge detectors such as Sobel, Prewitt, Robert and Laplacian of Gaussian (LoG) are already implemented using XSG.

[5] [Oluwayomi Adamo Saraju P. Mohanty Elias Kougianos] In this paper, author presented architecture and a hardware efficient FPGA based watermark module towards the development of the complete digital camera.

PROPOSED WORK

The entire operation will propose using Simulink and Xilinx blocks goes through three phases,

- Image pre-processing blocks.
- Edge enhancement algorithm using XSG.
- Image post-processing blocks

The design flow of hardware implementation of point processing operation using XSG is given in fig 1.Image source and image viewer are simulink block sets by using these blocks image can give as input and output image can be viewed on image viewer block set. Image pre-processing and image post-processing units are common for all the image processing applications which are designed using Simulink block sets. Point processing algorithm is different for each and every algorithm which is implemented using Xilinx System Generator block sets.

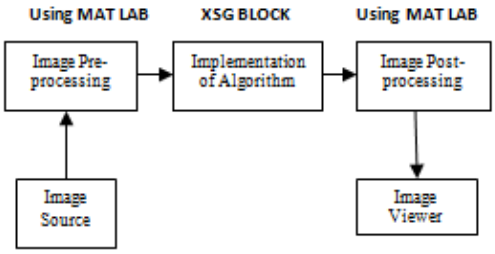


Fig 1: Design flow of hardware implementation of point processing operation

A. Image pre-processing blocks*:*

Image pre-processing in Mat lab helps to provide input to FPGA as specific test vector array which is suitable for FPGA Bit stream compilation using system generator.

• Resize: Resize block set input dimensions for an image.

• Convert 2-D to 1-D: image is converted into single array of pixels.

• Frame conversion and buffer: It is used to setting sampling mode and buffering of data.

The model based design used for image pre-processing is shown in Fig 2. Input images which may be color or grayscale are provided as input to the File block.

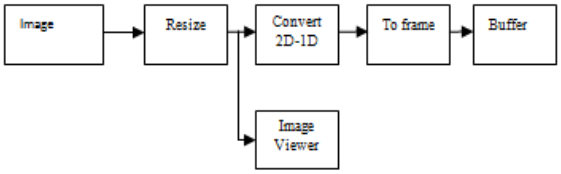


Fig 2: Image Post-processing Block

B. Image post processing blocks:

Image post processing helps to recreate image from 1D to 2D

- Data type conversion: Data type conversion converts image signal to unsigned integer format.
- Buffer: Buffer converts scalar samples to frame output at lower sampling rate.
- Convert 1D to 2D: Convert 1D image signal to 2D image matrix.

- Sink: Sink is used to display the output image back on the monitor.

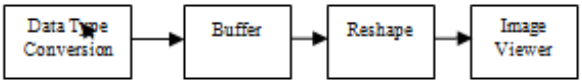


Fig 3: Image Post-processing block

CONCLUSION

Xilinx System Generator is very useful tool for developing computer vision algorithm. The technique implemented in this project will performs robust segmentation through a simple & efficient thresholding, which enables high performance with low use of computational resources.The result given in this work proves that the proposed hardware implementation of point processing operation gives optimal result for all kind of images which is used for various application.

Point processing algorithms using Xilinx System Generator can be extended to applications like background estimation in video, image filtering both in spatial and frequency domains and digital image watermarking applications, etc. The implementation further can be extended to area processes and frame processes in the field of digital image processing. The above experiments may also be performed with hardware-in-the loop verification and co-simulation approaches.

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