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DESIGN AND IMPLEMENTATION OF CASCADE H BRIDGE MULTILEVEL INVERTER

ASHISH MESHRAM[1], GERALDINE MATHEW[2], SARANG THAKRE[1]

1. Electrical Department, KDKCE, Nagpur
2. Assistant Professor, Electrical Department, KDKCE, Nagpur

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Abstract: Now a days supplying high quality power to the critical loads like medical equipment, research instruments etc is a vital importance. The distortion of the output voltage decreases as the number of level increases and it is further improved by applying pulse width modulation (PWM) techniques. This paper deals with the working of a cascade H bridge multilevel inverter using PWM switching technique. The simulation and its output are respectively presented.

Keywords: Cascade, H Bridge, multilevel, PWM, inverter

Corresponding Author: MR. ASHISH MESHRAM

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INTRODUCTION

The multilevel inverter has gained much attention in recent years due to its advantages in high power with low harmonics applications. The general function of the multilevel inverter is to synthesize a desired high voltage from several levels of dc voltages that can be batteries, fuel cells, etc.

In recent years the Multi-Level Inverters are very popular for Industrial and powers system applications due to their advantages on Two-level inverters i.e. High Power rating, Low Harmonics so they give the higher efficiency. The different topologies of Multi-Level Inverters are Neutral-point clamped (NPC) or Diode Clamped (DC) inverter, Flying capacitor inverter and Cascade inverter. As the level increases, NPC require more clamping diodes so the control of real power flow becomes very difficult. In flying capacitor inverter as the level increases, number of storage capacitors also increases hence they become bulky and costly; there are more switching losses in this topology. The cascaded multilevel inverters have more advantages than other topologies, because it does not require any balancing capacitors and diodes. Cascaded inverters need separate DC sources for each H-Bridge, so there is no voltage balancing problem, but isolated DC sources are not readily available, this is the main drawback of this topology. In this paper Cascade H Bridge Inverter is studied for PWM control scheme.

II. MULTILEVEL INVERTER

In 1975, the concept of multilevel converters was first introduced. Multilevel means that the inverter can generate more output voltage levels than those of the common three- level converter. Subsequently, several multilevel converter topologies have been developed. The basic principle of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected. Fig. 1 shows a multilevel inverter topology example. Each separate dc source (SDCS) is connected to a single-phase full-bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, + Vdc, 0, and - Vdc by connecting the dc source to the ac output by different combinations of the four switches, S1, S2, S3, and S4.To obtain + Vdc, switches S1 and S4 are turned on, whereas - Vdc can be obtained by turning on switches S2 and S3. By turning on S1 and S2 or S3 and S4, the

output voltage is 0. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate dc sources. The AC outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The phase voltage Van=Va1+⋯+Va[(m-1)/2]

A. Cascade H bridge multilevel inverter

The Cascaded H-Bridge (CHB) Multi Level Inverter (MLI) is a cascade of H-Bridges, or H-Bridges in a series configuration. A CHB MLI consists of a string of H-Bridge (single-phase full bridge configuration) inverter units in each of its three phases. An example of a CHB MLI is shown. The three-level converter has the same configuration as a single H-Bridge inverter, a single phase full bridge inverter used in PWM. The four switches S1, S2, S3 and S4 are operated within limits to generate three discrete outputs Vab with levels of - vdc, 0 or + Vdc.

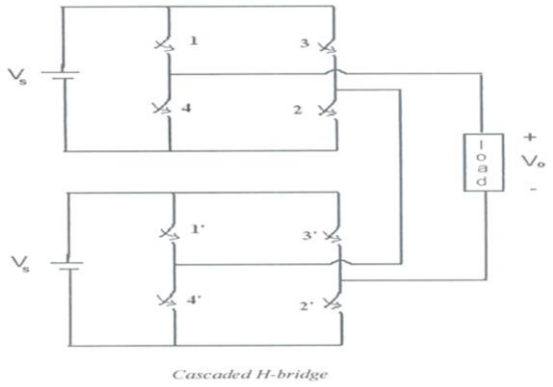

Figure 1 Multilevel inverter topology (cascade H bridge)

When S2 and S3 are on the output is-Vdc, when either pair S1 and S2 or S3 and S4 are on the output is 0, and when S1 and S4 are turned on the output is +Vdc. The simplest inverter i.e. a H-Bridge inverter is illustrated in (Fig. 2). A cascaded multilevel inverter is made up from a series of H-bridge (single-phase full bridge) inverters, each with their own isolated dc bus. This multilevel inverter can generate almost sinusoidal waveform voltage from several separate dc sources (SDCSs), Fig 2 shows a single phase structure of an M-level H-bridges multilevel cascaded inverter. Each level can generate three different voltage outputs +Vdc,0,-Vdcc by connecting the dc sources to the ac output side by different combinations of the four switches.

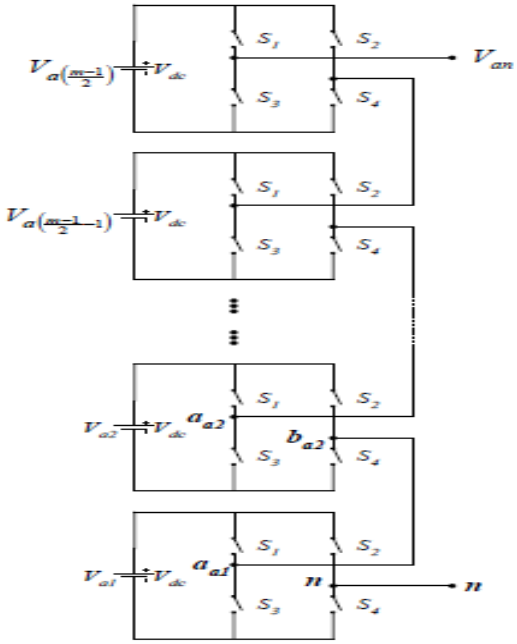

Figure 2 Cascade H bridge m level multilevel inverter

B. Switching Table for Nine Level Cascaded Multilevel Inverter

Table 1 shows the voltage levels and their corresponding switch states for the positive half cycle of the output voltage. State condition 1 means the switch is on and 0 means the switch is off. Each switch is turned on only once per cycle and therefore reduces switching losses.

TABLE I: OUTPUT VOLTAGES AND THEIR CORRESPONDING SWITCHING STATES

	Output Voltage V0			
Output	$V1$	$V1+V2$	$V1+V2+V3$	$V1+V2+V3+V4$
M11	1	1	1	1
M12	1	1	1	1
M13	0	0	0	0
M14	0	0	0	0
M21	0	1	1	1
M22	1	1	1	1
M23	0	0	0	0
M24	0	0	0	0
M31	0	0	1	1
M32	1	1	1	1
M33	0	0	0	0

M34	0	0	0	0
M41	0	0	0	1
M42	1	1	1	1
M43	0	0	0	0
M44	0	0	0	0

III. PULSE WIDTH MODULATION TECHNIQUE

Because of advances in solid state power devices and microprocessors, switching power converters are used in industrial application to convert and deliver their required energy to the motor or load. PWM signals are pulse trains with fixed frequency and magnitude and variable pulse width. There is one pulse of fixed magnitude in every PWM period. However, the width of the pulses changes from pulse to pulse according to a modulating signal. When a PWM signal is applied to the gate of a power transistor, it causes the turn on and turns off intervals of the transistor to change from one PWM period to another PWM period according to the same modulating signal. The frequency of a PWM signal must be much higher than that of the modulating signal, the fundamental frequency, such that the energy delivered to the motor and its load depends mostly on the modulating signal. The pulses of a symmetric PWM signal are always symmetric with respect to the center of each PWM period. The pulses of an asymmetric PWM signal always have the same side aligned with one end of each PWM period. It has been shown that symmetric PWM signals generate fewer harmonics in the output currents and voltages. The advantages possessed by PWM techniques are Lower power dissipation, Easy to implement and control, No temperature variation and aging-caused drifting or degradation in linearity, Compatible with today's digital micro-processors, the output voltage control can be obtained without any additional components and with the method, lower order harmonics can be eliminated or minimized along with its output voltage control. As higher order harmonics can be filtered easily, the filtering requirements are minimized. The main disadvantage of this method is that SCRs are expensive as they must possess low turn-on and turn-off times.

A. Single pulse width modulation

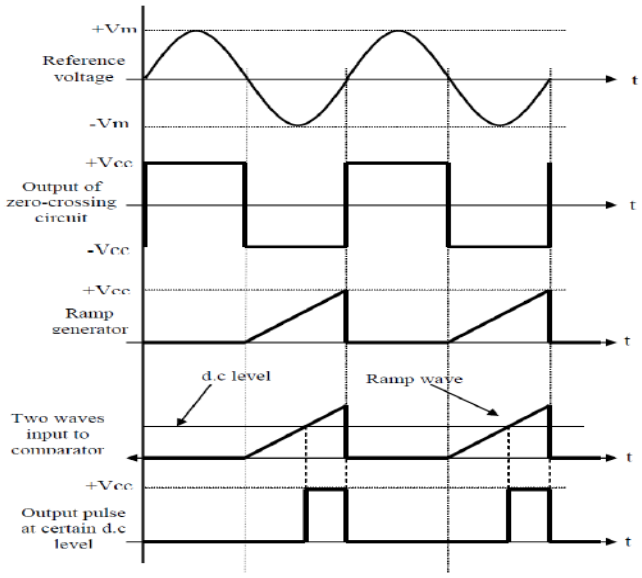

Figure 3 The generation of gating signals of single pulse width modulation

In single pulse-width modulation control, there is only one pulse per half-cycle and the width of the pulse is varying to control the output voltage. Fig.-3 shows the generation of gating signals of single pulse width modulation. The gating signals are generated by: The single pulse-width modulation converts the reference signal to the square wave signal. This process is obtained by comparison of the reference signal to the zero-crossing circuit to get desired pulse for the switch to be turned on, only the positive part of the input signal covers positive part of the output signal (square wave) and later it compares negative part for getting the required pulses for switches to be triggered as shown in figure. 3.

SIMULATION RESULT

A. Simulation of Cascaded Multilevel Inverter

The simulation model of the proposed nine level cascaded multilevel inverter system for various PWM techniques is shown in fig 4. This circuit comprises four single phase bridges connected in cascade and MOSFET switches are used. Four separate voltage sources of vaue Vdc=90V is used to energize the power circuit. The load on the inverter is resistive of value R= 50 ohm. Simulation of power circuit is carried out using control circuit which generates required gating signals. Three different PWM techniques are used to produce the gating signals. Using this signal, the output voltage and current waveforms are obtained and the corresponding frequency spectrum is also analyzed.

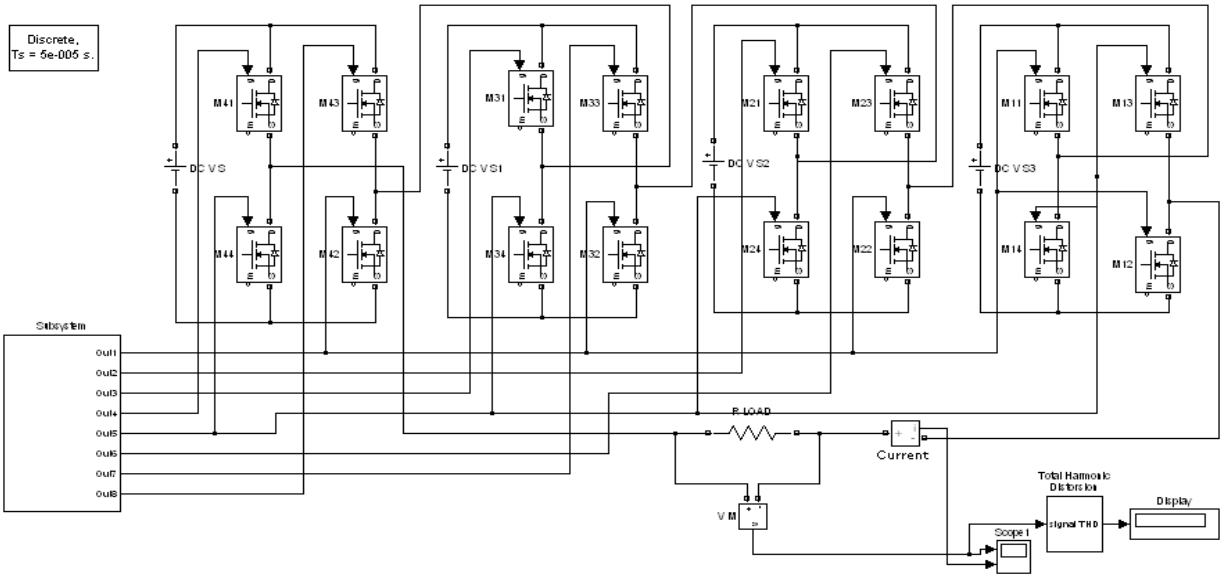

Figure 4 Simulink model for nine-level cascaded multilevel inverter

B. Output of PWM unit

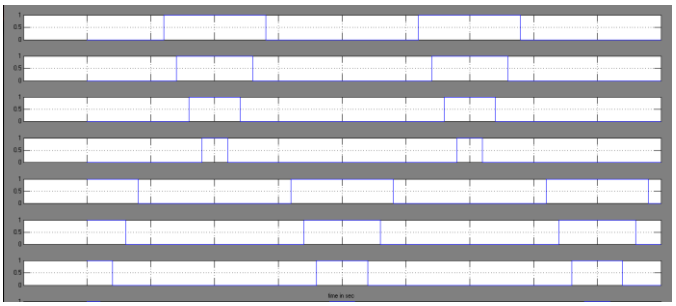

Figure 5 Gating pulses for various switches in single PWM

C. Output voltage of a nine-level cascaded multilevel inverter system

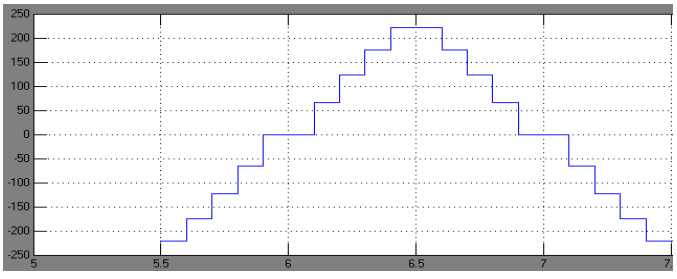

Figure 6 Simulated output voltage waveform of a multilevel inverter

Figure shows output voltage vs time graph, Output shown in fig. 6 is a stepped output of a peak to peak nine steps multilevel inverter. The stepped output reduces the voltage stress and thus enhances the quality of the voltage by comparatively reducing harmonics.

V. CONCLUSION

A simulation model for cascaded H bridge multilevel inverter is developed using MATLAB platform. The paper presents the main circuit of multilevel inverter using PWM switching technique simulation results in details. With increase in number of steps in multilevel inverter the harmonics considerably reduces.

REFERENCES

1. Haiwen Liu, Leon M. Tolbert, Surin Khomfoi, Burak Ozpineci, Zhong Du, “Hybrid Cascaded Multilevel Inverter with PWM Control Method”, IEEE 2008, pp162-169

2. P. Maruthu Pandi, N. Devarajan, “Comparative Analysis of Power Quality Issue in Cascaded Multilevel Inverter Using PWM Techniques”, European Journal of Scientific Research ISSN 1450-216X Vol.60 No.3 (2011), pp.458-468.

3. Bindeshwar singh, Dr.K S Verma, “Multilevel inverter:A literature survey on topologies and control strategies”, IJRIC Vol.10 31st july 2012.pp 7-14.

4. L. M. Tolbert, F. Z. Peng, “Multilevel converters as a utility interface for renewable energy systems,” in Proceedings of 2000 IEEE Power Engineering Society Summer Meeting.pp1271-1274.

5. K.Surya Suresh and M.Vishnu Prasad, “Analysis and Simulation of New Seven Level Inverter “, International Journal of Scientific and Research Publications, ISSN 2250-3153 Volume 2, Issue 4, April 2012, pp 1-6.

6. F. Z. Peng, J. W. McKeever, D. J. Adams, “Cascade mult ilevel inverters for utility applicat ions,” IEEE IECO, vol. 2, July 2000.pp 437-442.

7. M. Kavitha, A. Arunkumar, N. Gokulnath, S. Arun, “New Cascaded H-Bridge Multilevel Inverter Topology with Reduced Number of Switches and Sources”, Journal of Electrical and Electronics Engineering (IOSR-JEEE) ISSN: 2278-1676 Volume 2, Issue 6 (Sep-Oct. 2012), PP 26-36

8. Divya Subramanian, Rebiya Rasheed, “Nine-Level Cascaded H-Bridge Multilevel Inverter”, International Journal of Engineering and Innovative Technology (IJEIT) ISSN: 2277-3754 Volume 3, Issue 3, September 2013, pp 201-205.

9. Murugesan.G, “A new multilevel inverter topology using less number of switches”, IJEST Vol. 3 No. 2 Feb 2011.pp1500-1510

10. Madhav D. Manjrekar Thomas A. Lipo, “A hybrid multilevel inverter topology for drive applications”, 1998 IEEE.