INTERNATIONAL JOURNAL OF PURE AND APPLIED RESEARCH IN ENGINEERING AND TECHNOLOGY

A PATH FOR HORIZING YOUR INNOVATIVE WORK

DESIGN OF LOW POWER MULTIPLIERS USING APPROXIMATE ADDER

MR. PAWAN SONWANE[1], DR. MRS. P. MALATHI[2]

1. Dept. of Electronics and Tele-Communication, D. Y. Patil College of Engg., Pune, India.
2. Professor & Vice-Principal, Dept. of Electronics and Tele-Communication, D. Y. Patil College of Engg., Pune, India

Accepted Date: 05/03/2015; Published Date: 01/05/2015

Abstract: Power consumption is a major issue for circuit design in CMOS technology. In most multimedia applications, human eyes can gather useful information from slightly imprecise outputs [1]. To reduce power consumption for applications in which strict exactness is not required, approximate implementations of a circuit have been considered as a potential solution. In imprecise computing, power reduction is achieved through the relaxation of accuracy. Previous research on logic complexity reduction have focused on gate, algorithm and logic levels. In this paper, as the alternative approach, we propose logic complexity reduction at the transistor level to take advantage of the relaxation of numerical accuracy. Addition is a fundamental operation for any digital signal processing and control system. We examined this concept by proposing approximate full adder cell and used them to design approximate Multiplier. In addition to the inherent reduction in switched capacitance, our techniques result in significantly shorter critical paths, enabling voltage scaling. The final approximation consisting of only ten transistors and was found to consume the least power of all reviewed designs. Power savings of up to 55% was achieved using the proposed approximate adders, when compared to accurate adders.

Keywords: Approximate adders, Mirror adder, Shifters, Multipliers

Corresponding Author: MR. PAWAN SONWANE

Access Online On:

www.ijpret.com

How to Cite This Article:

Pawan Sonwane, IJPRET, 2015; Volume 3 (9): 449-459

PAPER-QR CODE

INTRODUCTION

Commonly digital signal processing (DSP) blocks are used as core in multimedia applications. Most of these DSP blocks, the ultimate output is either an image or a video. The limited perception of human vision allows the outputs of these algorithms to be numerically approximate rather than accurate [2]. This numerical exactness relaxation provides some freedom to perform imprecise or approximate computation. The development simplified imprecise arithmetic units can provide an extra layer of power saving over conventional low-power designs. The adder is one of the most critical components of any DSP, as it is profitable in the floating-point unit, in the Arithmetic Logic Unit (ALU) and for address generation in case of cache or memory access. Now a day's low power consumption along with minimum area and delay requirements is one of important design consideration for IC designers.

Some researches that focus on low-power design by approximate computing at the algorithm and architecture levels include nonuniform voltage overscaling (VOS) [10], significance driven computation (SDC) [7-9] and algorithmic noise tolerance (ANT) [3-6]. All reviewed techniques are based on the concept of VOS, coupled with additional circuitry for limiting and correcting the resulting errors.

We propose a novel 10 transistor approximate adder circuit which will be used to design the approximate multipliers. A reduction in logic complexity is accomplished at transistor level by removing some of the transistors required in the accurate adder design. Additionally, the node capacitances are reduced to lower the power/energy consumption of the proposed circuits. In this paper, energy consumption, area, delay, and power-delay product are measured for comparing the different designs with an accurate multiplier.

A similar work appeared in [1]. We extend the work proposed in [1] by giving one more simplified version of the MA. Our contributions in this paper are summarized as follows.

- To simplify the logic complexity of a conventional MA cell by reducing the number of transistors and switched capacitances.
- To design array multiplier by using approximate adders.
- We will compare accurate multiplier, inaccurate multiplier designs based on parameters energy consumption, area, delay, and power-delay product.

In summary, our aim is to target low-power design using simplified and approximate logic implementations. Our work differs from other works significantly (SDC, ANT, and non-uniform

VOS) since we exploit error resiliency using different approach. Since DSP blocks mainly consist of adders and multipliers (which are, in turn, built using adders), We propose logic complexity reduction at the transistor level. We apply this to addition at the bit level by simplifying the mirror adder (MA) circuit. We develop imprecise but simplified multipliers, which provide an extra layer of power savings over conventional low-power design techniques. Complexity reduction leads to power reduction in two different ways.

- An inherent reduction in switched capacitance and leakage results from having smaller hardware.
- Complexity reduction frequently leads to shorter critical paths, facilitating voltage reduction without any timing-induced errors**.**

I. APPROXIMATE ADDERS

In this section we will discuss various methodologies for designing approximate adders. We have reviewed previous work in same domain [1]. We will propose some new approximation strategies as an addition to them. Mirror adder (MA) is most widely used implementation of full adder (FA). Since, MA is transistor level implementation of FA, we will use MA as basic building block for proposing new design.

1. Conventional Mirror Adder

The figure 1 below shows conventional mirror adder. This MA consist of 24 transistors. It functions similar to the FA.

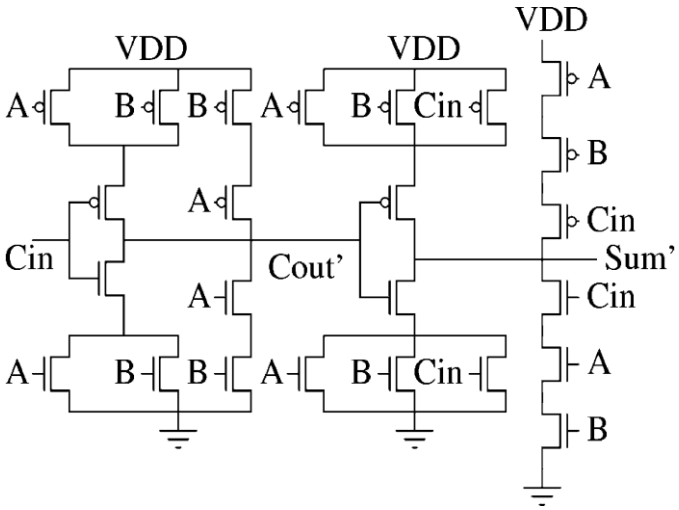

Fig 1. Conventional Mirror Adder [1]

Previous work in same domain [1] proposed various approximations. Those all approximations reduce number of transistors used in the MA, but also introduces some error in them.

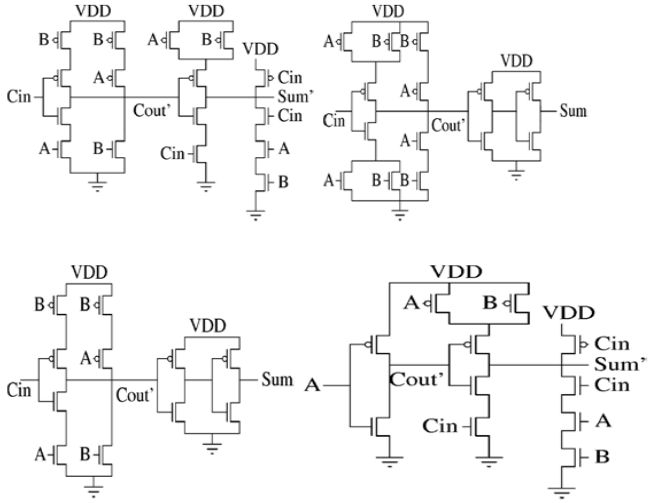

Fig 2. All Approximations proposed in [1]

Fig. 2 shows all the approximation that are referred. The Fig. 3 shows the truth table for conventional adder and approximations 1-4 [1].

Inputs			Accurate Outputs		Approximate Outputs							
A	B	C_{in}	Sum	C_{out}	Sum_1	C_{out1}	Sum_2	C_{out2}	Sum_3	C_{out3}	Sum_4	C_{out4}
0	0	0	0	0	0 ✓	0 ✓	1 ×	0 ✓	1 ×	0 ✓	0 ✓	0 ✓
0	0	1	1	0	1 ✓	0 ✓	1 ✓	0 ✓	1 ✓	0 ✓	1 ✓	0 ✓
0	1	0	1	0	0 ×	1 ×	1 ✓	0 ✓	0 ×	1 ×	0 ×	0 ✓
0	1	1	0	1	0 ✓	1 ✓	0 ✓	1 ✓	0 ✓	1 ✓	1 ×	0 ×
1	0	0	1	0	0 ×	0 ✓	1 ✓	0 ✓	1 ✓	0 ✓	0 ×	1 ×
1	0	1	0	1	0 ✓	1 ✓	0 ✓	1 ✓	0 ✓	1 ✓	0 ✓	1 ✓
1	1	0	0	1	0 ✓	1 ✓	0 ✓	1 ✓	0 ✓	1 ✓	0 ✓	1 ✓
1	1	1	1	1	1 ✓	1 ✓	0 ×	1 ✓	0 ×	1 ✓	1 ✓	1 ✓

Fig 3. Truth table for conventional adder and approximations 1-4 [1]

The truth table above shows the tick marks for right outputs and cross for wrong outputs.

2. Approximation 6: Adder with 10 Transistors

All the reviewed approximations contain some errors in sum and/or carry output as we have discussed[1].Since, such approximations deteriorates the quality of the output to some extent, they may not serve the purpose even though they reduce power to about 69% [1]. Hence, we worked in the manner to propose a new design with less number of transistors as well as errors. We developed a new design of MA which has only 10 transistors and it produces correct output similar to conventional MA. Note, that the approximate arithmetic units not only have a

reduced number of transistors, but care is taken to ensure that the internal node capacitances are greatly reduced. The proposed adder is shown in fig 4.

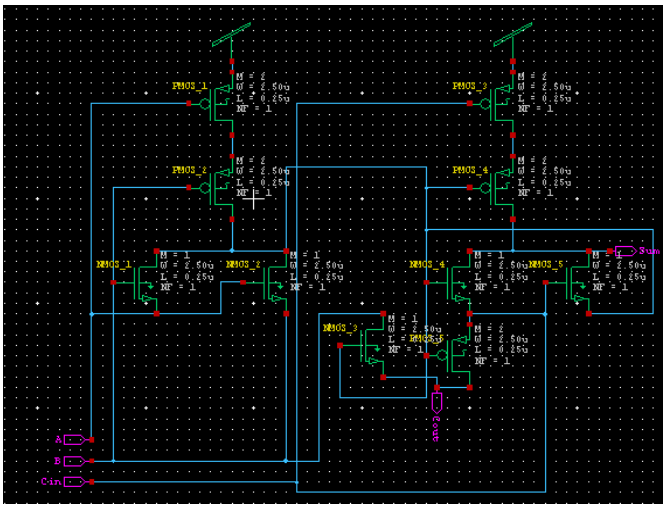

Fig 4: Schematic of adder with 10 transistors

Fig. 4 shows the schematic of adder with 10 transistors and following figure (Fig. 5) shows the outputs of the proposed design.

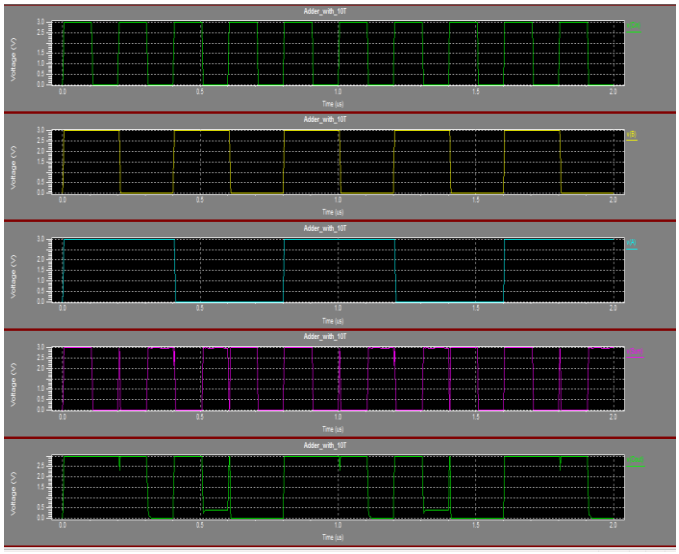

Fig 5: Output of adder with 10 transistors

II. 4 BIT ARRAY MULTIPLIERS USING ADDER

The adder is one of the most critical components of any DSP, as it is profitable in the floating-point unit, in the Arithmetic Logic Unit (ALU) and for address generation in case of cache or memory access. To demonstrate the efficacy of the proposed adder, we designed the multipliers using adder [13]. We compare the two designs, one with conventional MA as a building block, second with the proposed adder with 10 transistors. The two designs are compared based on the performance parameters like propagation delay, number of transistors and power dissipation.

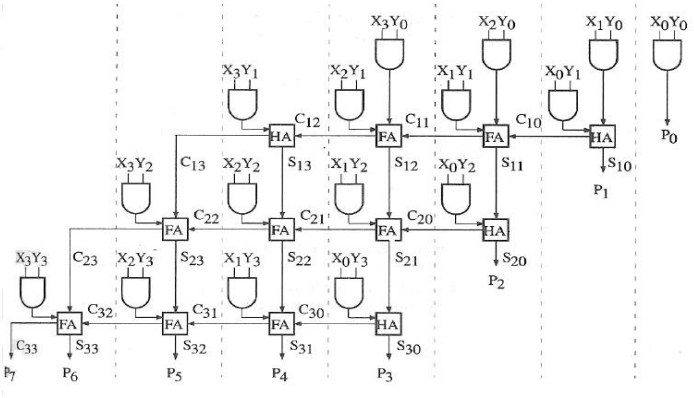

Fig 6: Design of 4-bit Array Multiplier

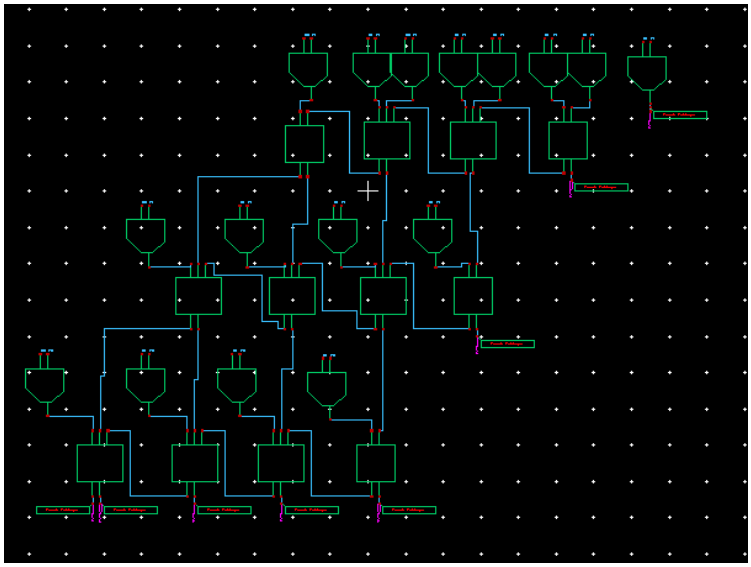

Fig 7: 4-bit Array multiplier using conventional MA

Figure 7 shows 4-bit array multiplier using conventional MA and following figure (Fig. 8) shows the output of the 4-bit array multiplier using conventional MA for the inputs Multiplicand = 1010 and Multiplier = 1010 with P1 is at bottom and P7 is attop**.**

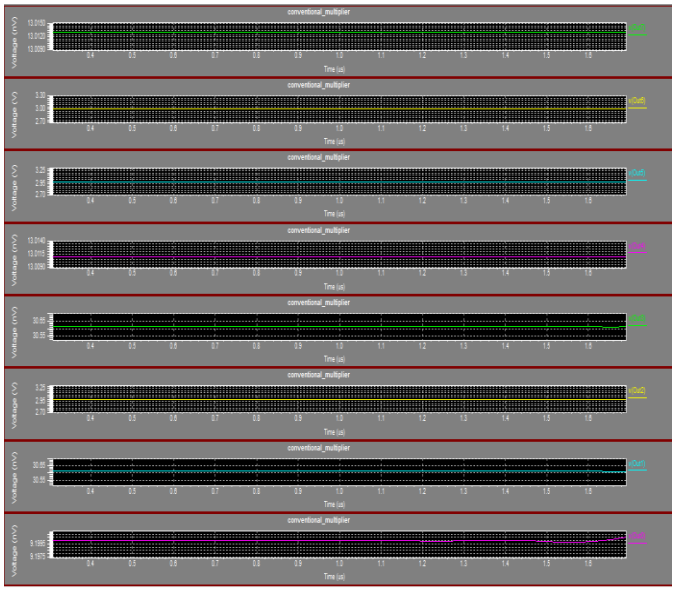

Fig 8: output of the 4 bit array multiplier using conventional MA

Now we will replace the conventional MA by proposed adder with 10 transistors and find out the results.

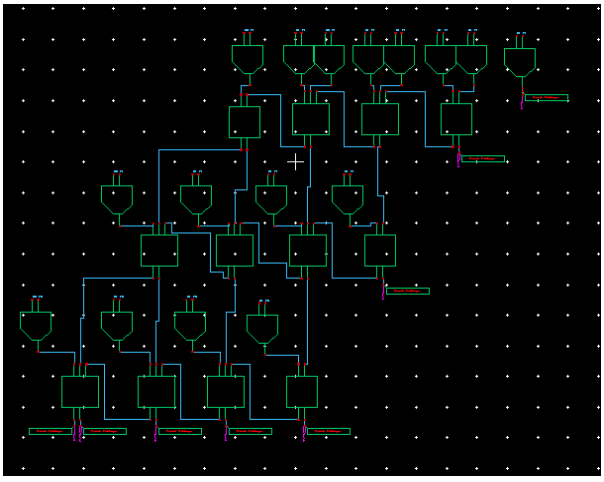

Fig 9: 4-bit Array multiplier using proposed adder

Schematic for array multiplier using conventional MA and the schematic for 4-bit Array multiplier using proposed adder (Fig. 9) are looking same as it is having symbolic view of the full adder, the inner designs are different for both. Following figure (Fig. 10) shows the output of the 4-bit array multiplier using proposed adders.

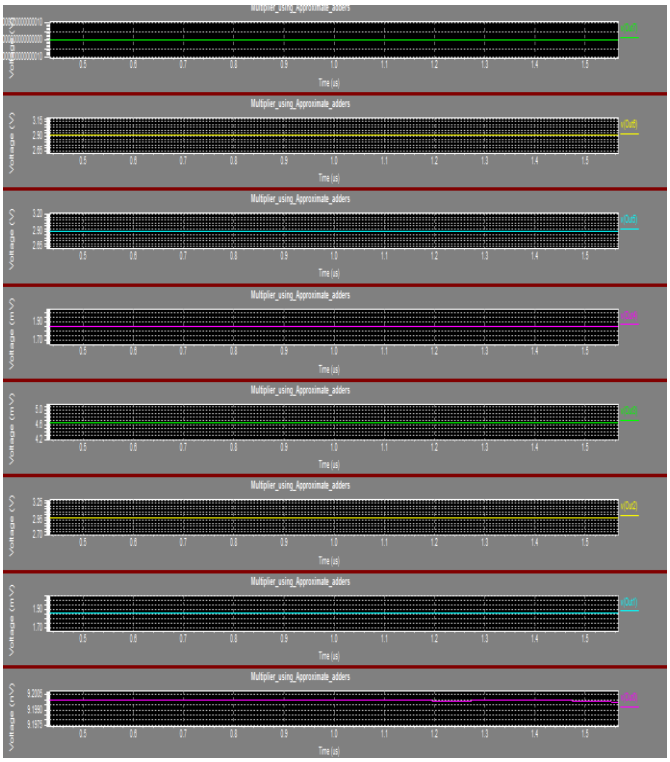

Fig 10: output of the 4-bit array multiplier using proposed adder

Figure 10 shows the output waveform of multipliers for the inputs Multiplicand = 1010 and Multiplier = 1010 with P1 is at bottom and P7 is at top.

III. RESULTS

The functionality of the multipliers is verified and their average delay, power, number of transistors and power delay product are calculated. Simulation waveforms are shown in Fig. 10 and Fig. 12 are the outputs of the multipliers designed at transistor level using S-Edit of TANNER EDA tool with 0.20 um technology at 35c temperature. The attention is not only on delay or power but also on the number of transistors used. We can achieve better performance in higher order circuits.

IV. PERFORMANCE PARAMETER AND SIMULATION SET-UP

Properties	Multiplier with Conventional MA	Multiplier with proposed Adder
Delay (nS)	10.79	8.67
Power(µW)	13.27	7.52
PDP (fJ)	143.18	65.19
No. of Trans	464	232

Table I: Comparison of performance parameters

The comparative results for two different 4-bit multipliers for different logic design styles are given in Table. I. To achieve desired performance, the circuits are designed using CMOS process in 90 nm technology. The 4-bit multipliers are compared based on the performance parameters like propagation delay, number of transistors and power dissipation. All the circuits have been designed using TANNER EDA v13.0 with model file as dual.md. To achieve low power and high performance multipliers these are tested at 5v so, that the performance of multipliers can be improved. The channel width of the transistors is 270nm for the NMOS and same for the PMOS. The output capacitance *CL* is 1pF in all cases whereas the operating frequency is 60MHz. Due to dependency on various parameters, the power estimation is a difficult task and has received a lot of attention [11]. T-spice is used in order to analyze the results [12].

VI. DISCUSSION AND CONCLUSION

In this paper, we have proposed an imprecise or approximate adders that can be utilized reduce power requirement of DSP systems. Our technique aimed to simplify the complexity of a conventional MA cell at transistor level and also the load capacitances. Note that our approach differed from previous approaches where errors were introduced due to VOS [3]–[10]. A decrease in the number of series connected transistors helped in reducing the effective switched capacitance and achieving voltage scaling. This procedure can be illustrated for many DSP applications in future, for examples, DCT and FIR filter. We believe that the proposed approximate adders can be used on top of already existing low-power techniques like SDC and ANT.

VII. ACKNOWLEDGMENT

The authors are pleased to acknowledge discussions with Dr. Khairnar, Prof & H.O.D, Dept. of ECE, D. Y. Patil college of Engg. Pune and Prof. (Dr.) Manish Sharma, P.G. coordinator (VLSI), D. Y. Patil college of Engg. Pune.

VIII. REFERENCES

1. Vaibhav Gupta, Debabrata Mohapatra, Anand Ragunathan, "Low Power Digital Signal Processing Using Approximate Adder", IEEE Transactions On Computer-Aided Design Of Integrated Circuits And Systems, Vol.32,No.1, January 2013.

2. P. Kulkarni, P. Gupta, and M. Ercegovac, "Trading accuracy for power with an under designed multiplier architecture", in Proc. 24th IEEE Internantional Conference VLSI Design, Jan. 2011, pp. 346–351.

3. R. Hegde and N. Shanbhag, "Energy-efficient signal processing via algorithmic noise-tolerance," in Pro IEEE/ACM Int. Symp. Low Power Electron. Design, Aug. 1999, pp. 30–35.

4. R. Hegde and N. R. Shanbhag, "Soft digital signal processing," IEEE Trans. Very Large Scale Integr. Syst., vol. 9, no. 6, pp. 813–823, Jun. 2001.

5. B. Shim, S. Sridhara, and N. Shanbhag, "Reliable low-power digital signal processing via reduced precision redundancy," IEEE Trans. Very Large Scale Integr. Syst., vol. 12, no. 5, pp. 497–510, May 2004.

6. G. Varatkar and N. Shanbhag, "Energy-efficient motion estimation using error-tolerance," in Proc. IEEE/ACM Int. Symp. Low Power Electron. Design, Oct. 2006, pp. 113–118.

7. D. Mohapatra, G. Karakonstantis, and K. Roy, "Significance driven computation: A voltage-scalable, variation-aware, quality-tuning motion estimator," in Proc. IEEE/ACM Int. Symp. Low Power Electron. Design, Aug. 2009, pp. 195–200.

8. N. Banerjee, G. Karakonstantis, and K. Roy, "Process variation tolerant low power DCT architecture," in Proc. Design, Automat. Test Eur., 2007, pp. 1–6.

9. G. Karakonstantis, D. Mohapatra, and K. Roy, "System level DSP synthesis using voltage overscaling, unequal error protection and adaptive quality tuning," in Proc. IEEE Workshop Signal Processing Systems, Oct. 2009, pp. 133–138.

10. Tanner EDA Inc. 1988, User_s Manual, 2005.

11. Najm, F., —A survey of power estimation techniques in VLSI circuits, ‖ IEEE Transactions on VLSI Systems, vol. 2, 1995, pp. 446-455.

12. Kang, S., —Accurate simulation of power dissipation in VLSI circuits, ‖ IEEE Journal of Solid-State Circuits, vol. 21, 1986, pp. 889-891.

13. Aditya Kumar Singh, Bishnu Prasad De, Santanu Maity, “Design and Comparison of Multipliers Using Different Logic Styles”, International Journal of Soft Computing and Engineering (IJSCE), Volume-2, Issue-2, May 2012