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LOW POWER SAR USING CMOS TECHNOLOGY; VLSI IMPLEMENTATION"

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Abstract: Successive Approximation analogtodigital converter implemented using CMOS technology with Low voltage. Improved design of ADC is presented here with low optimal delay and low power consumption by using double edge triggered T-flip flops (DETTFF).This design is suitable for standard CMOS technology with low power ,low cost VLSI implementation.

Keywords: Analog to digital converter, Comparator, VLSI, SAR, DAC.

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INTRODUCTION

In a recent survey article on data conversion, it was pointed out that the most popular type of analog-to-digital (A/D) converter in use today is the one employing the successive-approximation (SA) logic. The main reason for its popularity lies in its inherently fast conversion time which is a constant n clock periods for an n-bit converter. When compared to other A/D schemes such as the dual-slope integrating method and the servo-type method, the successive-approximation scheme offers much higher conversion rates .Basically, the successive-approximation A/D converter consists of three main components an analog comparator, a DAC, and a successive-approximation register (SAR) all of which are connected in feedback as shown in the circuit1.

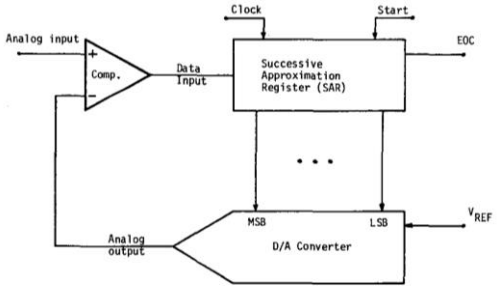


Fig. 1. Successive-approximation A/D converter.

In a conventional single edge-triggered (SET) flip- flop, data moves from input to output in synchrony with one edge of the clock. The use of double edge-triggered flip-flops has been already proposed for low-power circuit design. In a DET flip-flop, both rising and falling edges of the clock signal are used to transfer data from input to output. In this way, for a given throughput, the clock frequency can be halved with respect to a system using SET flip- flops, with a reduction of power consumption. Unfortunately, DET flip-flops require a more complex implementation with respect to SET flip flops. This results not only in larger silicon area but also requires higher number of internal nodes and transistors

II.Literature summary &related work

[1]In this paper, SAR uses a separate sequencer and code register made from D-type flip flop. This designing gives the advantage of simplicity and ease in construction. It consists of reproducing each bit cell containing only two D-type flip flops. Here sequencer operates synchronously with the clock input and the code register operate asynchronously since the clock input to the particular flip flop is obtained from the output of succeeding flip flops. In this

design, 3 flip flop delay occurs between the leading clock edge and the Output of the code register. As the number of flip flop increases, the power requirement is also high. single D flip flop is used in each bit cell which functions both as sequencer and code register. This design is often referred as the sequencer/code register design. However it is necessary to add some steering logic in order to control the clock and data inputs to each cell. This designing is having the advantage of Less number of flip flops are needed for designing and power consumption is low as compared to previous one. It is having some of the disadvantages like the complex steering logic is needed, whose designing is a tedious job. It also introduces delay in the processing .In this design two extra flip flops are required i.e. n+2 for n bit conversion. One for holding the parallel data output and other for generating EOC signal.

[2] In this paper, Yuen studied the research done by Anderson and Russell and proposed his own model. According to Anderson, the SAR converter consists of number of identical cells, each containing a J-K flip flop with two AND gates. Russell's design makes the use of (n+2) D-Flip-Flops; this design requires more than two gates per cell. His design includes modification of Anderson's design and idea in Russell's design regarding the enabling of clock. Instead of two AND gates per cell, his model needs two OR gates. Following figure shows the proposed model of SAR. There are (n+1) J-K flip-flops one for each bit of the digital output and an extra one to signal completion. As we are using OR gates instead of AND gates, there is reduction in the complexity of the design as OR gates are easier to fabricate than AND gates. As J-K flip flops needs more power for its operation compared to D flip flops, the overall power requirement for the whole circuit increases. Asynchronous clock introduces the more delay in circuit operation.

3] In this paper, the design consists of N=6 J-K flip flops used both as a shift register and code register with k inputs fed by comparator output. The single row solution based on JK-Flip flops does not provide the expected benefits in terms of power consumption. It uses the asynchronous feedback through the AND gates which severely limits the maximum clock frequency.

[4] This paper compares two previously published Double Edge Triggered D Flip-flops (DETDFF) with the proposed design for their performance and power consumption. In Gago's DETTFF at negative edge of the clock, the upper circuit operates and issues the output and at positive edge of the clock, the lower circuit operates and gives the output. The circuit requires total 22 transistors. As the number of transistors is more, power consumption is more. In Waichung's DETDFF, At negative edge of the clock, the left stage issuing the output. At positive edge of the clock, the right stage issuing e output. When one stage is in action, the other stage is

deactivated. The circuit requires total 26 transistors. Here also the number of transistors is more, so power consumption is more.

III. Types of SAR:

1. Flash ADC:-

Sometimes called parallel ADC, is the fastest type of converter, but has limited resolution, high power dissipation and relatively large chip size. The main reason for the high power consumption is the large number of comparators. For an N-bit converter, we would need (2N-1) comparators, this means that the number of comparators increases exponentially with the number of bits.

2. SAR ADC:-

Successive approximation Register ADC represents the majority of the ADC market for medium to high resolution. This topology requires just one comparator; an N-bit SAR ADC will require N comparison periods and will not be ready for the next conversion until the current one is complete.

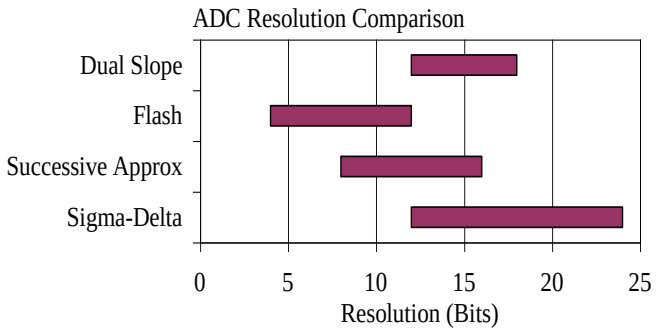
3. Sigma-Delta ADC:-

Sigma-Delta ADC contains very simple analog electronics (a comparator, voltage reference, a switch and one or more integrators and analog summing circuits), and quite complex digital computational circuitry. Sigma-delta converters trade speed for resolution.

3. Dual Slope converter:-

The sampled signal charges a capacitor for a fixed amount of time By integrating over time, noise integrates out of the conversion. Then the ADC discharges the capacitor at a fixed rate while a counter counts the ADC's output bits. A longer discharge time results in a higher count.

ADC Types Comparison



Type	Speed (relative)	Cost (relative
Dual Slope	Slow	Med
Flash	Very Fast	High
Successive Approximation	Medium – Fast	Low
Sigma-Delta	Slow	Low

IV. Analysis of problem:-

From the comparative study of different SAR logic, a problem is that the complexity, power and delay get increased. So there is a need to design a successive approximation register (SAR) having low optimal delay and low power consumption by using double edge triggered T-flip flops (DETTFF).

V. Objectives:

1. Low Cost& voltage: operate at small voltage and at low cost.

2. Low optimal delay: aim to reduce the delay.

3. Speed of operation: To achieve the high speed performance.

4. Low power: To achieve the Low power consumption.

VI. Desired implications:-

- As we are using T Flip flops, the power requirement for it is less as compared to other Flip flops.
- We are using double edge triggered Flip flops so the required clock period reduces to half and we will certainly get the increase in speed of operation.

- The designing of SAR by using DETTFF and the effective logic will certainly improves the performance of SAR in respect of speed and power consumption.

VII. How SAR ADC Works:

The SAR-ADC (Figure 1) captures an analog voltage signal, converts that signal to a digital word. The analog signal is captured with either an external sample/hold device or the SAR-ADC's internal sample/hold function. The SAR-ADC compares this input voltage to known fractions of the converter's external or internal voltage reference (VREF). At the input of a SAR converter, the input signal first sees a switch. Notice, that a closed switch creates a switch resistance (RIN) in series with a capacitive array. The top side of these capacitors connects to the inverting input of a comparator. The bottom side can tie into the input voltage, the voltage reference (VREF), or ground (V–). Initially, the bottom side connects to the input signal, VS. Once the capacitive array completely acquires the input signal, the input switch (S1) opens and the converter starts the conversion process.

During the conversion process, the bottom side of the MSB capacitor connects to VREF while the other capacitors connect to V– (or system ground). This action redistributes charge among all the capacitors. The comparator's inverting input moves up or down in voltage according to charge balancing. If the voltage at SC is greater than half VREF, the converter assigns "0" to the MSB and transmits that value out of the serial port. If this voltage is less than half VREF, the converter transmits a "1" out of the serial port, and the converter connects the MSB capacitor to V–. Following the MSB assignment, this process repeats with the MSB-1

VIII. Proposed work.

The design will be developed in the following modules,

1. DAC Design

In this module we would be designing a DAC with the same number of bits as the ADC. This will make sure that the designed DAC works faster and gives efficient outputs

2. Comparator Design

In this module, a comparator would be designed to compare the output of DAC with the actual analog signal, so that the further stages can work

3. SAR Register design

In this module, the SAR circuit would be developed an tested

4. System integration

In this module, Modules 1, 2 and 3 would be combined to develop the entire SAR ADC

5. Testing and optimization

In this module, the entire design would be tested and optimized if needed.

CONCLUSION:

High performance ADC is essential in wide range of applications such as data acquisition, measurement, and digital communication system. We are going to design one of good type of ADC, developed in >18 um process & its performance is compared with other propose ADCs on trade of resolution , speed , area , power consumption, supply voltage etc along with the key parameters requirements.

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