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DESIGN OF TREE MULTIPLIER USING REVERSIBLE LOGIC GATE

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Abstract: Reversible logic is one of the most vital issue at present time and it has different areas for its application, those are quantum computing, low power CMOS, DNA computing, nanotechnology, cryptography, digital signal processing (DSP), communication, computer graphics, quantum dot cellular automata. It is not possible to realize quantum computing without implementation of reversible logic. The reversible logic is designed with the significance to decrease depth of the circuits, the number of garbage outputs and quantum cost. This paper provides the basic reversible logic gates. These logic gates can be used for designing of more complex system having reversible circuits as a primitive component and which can execute more complicated operations using quantum computers. The basic building block of quantum computers are formed by reversible circuits because all quantum operations are reversible. The data relating to the primitive reversible gates which are available in literature and helps researches in designing higher complex computing circuits using reversible gates. In this paper tanner tool is used for simulation result.

Keywords: Reversible logic gate, Wallace unsigned multiplier, Reversible circuit.

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INTRODUCTION

The reversible logic operations do not erase (lose) information and dissipate very less heat. Demand of reversible logic is high in high speed power aware circuits. Interest of reversible circuit is high in nanotechnology, quantum computing optical computing and low power CMOS design. Application of reversible logic is very high in quantum computers. Quantum network (or a family of quantum networks) can be viewed as a quantum computer. Quantum network can be consists of quantum logic gates; each. An elementary unitary operation on one, two or more two–state quantum systems called qubits is performed by each gates. An elementary unit of information corresponding to the classical bit values 0 and 1 is represented by each qubit is reversible, Quantum networks effecting elementary arithmetic operations such as addition, multiplication and exponentiation cannot be directly deduced from their classical Boolean counterparts (classical logic gates such as AND or are clearly irreversible) because any unitary operation is reversible. Thus, reversible logic Components can be made from quantum arithmetic. Serious problems for today's computer chips are heat generation and power dissipation.

The 30-year-long trend in microelectronics has been to increase both speed and density by scaling of device components. In the last decade the heat generation is reduced by higher level of integration and new fabrication processes during this trend. Quantum gates which are represented by unitary matrices have potentials to implement reversible logic circuits. A valid Quantum operation is represented by each quantum gate. Each quantum gate must be unitary and hence must be reversible. Many classical logic gates are irreversible but quantum gates are reversible.

REVERSIBLE LOGIC GATE:

If n is input and m output is logic gate and there is a one-to-one correspondence between its inputs and outputs, and then this type of logic gate is called to be reversible.

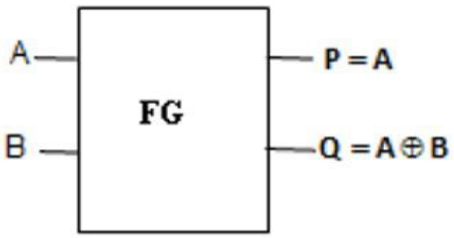
If and only if the (Boolean) function is bijective then the gate is said to be reversible. In other words, a gate is reversible if each of its input vector maps into a unique output vector and vice versa

Following are basic reversible logic gates. Truth table of reversible gate is shown below.

a) Feynman gate :

The Feynman gate which is a 2*2 gate and is also called as Controlled NOT and it is widely used for fan-out purposes.

The inputs (A, B) and outputs P=A, Q=A XOR B.

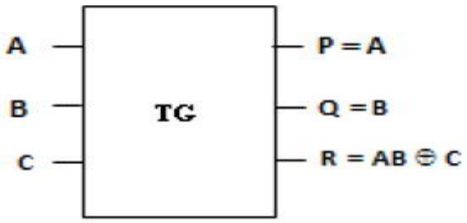


Truth table of Feynman gate:

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

b) Toffoli gate :

Toffoli gate which is a 3*3 gate with inputs (A, B, C) and outputs P=A,Q=B, R=AB XOR C.



Truth table of toffoli gate:

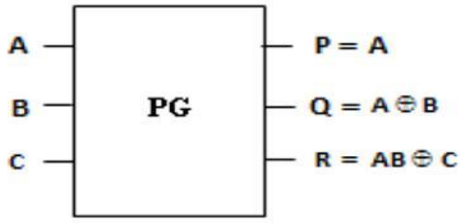
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0

1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

c) Peres gate :

Peres gate which is a 3*3 gate having inputs (A, B, C) and outputs

P = A; Q = A XOR B; R = AB XOR C.



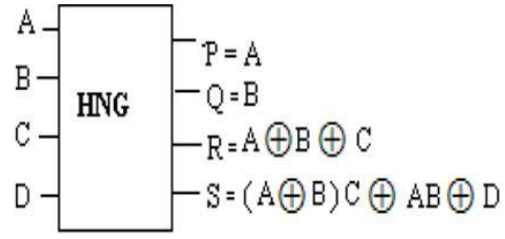
Truth table of peres gate:

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

d) Haghparast Navi gate:

Each output is annotated with the corresponding logic expression. It is 4*4 gate having inputs(A,B,C,D) and output P=A,Q=B,

R=AB XORC,S=(A XOR B)C XOR AB XOR D.



This paper proved that the proposed multiplier is better and optimized, compared to its existing counterparts with respect to the number of gates, constant inputs, garbage outputs, hardware complexity, and number of transistors required.

By using full adders and half adders in their reduction phase. This paper presented that Wallace high-speed multipliers half adders do not reduce the number of partial product bits. Hence, reduction in the hardware complexity can be achieved by the number of half adders used in a multiplier reduction. This paper proposed a novel reversible multiplier and the aim of this paper was decrease the depth of the circuit. The proposed in this paper the depth of novel reversible multiplier is less and quantum cost is not increase or the number of garbage outputs with respect to previous counterparts. In proposed design, using Peres gates partial products were generated.

This paper provided the initial threshold to building of more complex system which can execute more complicated operations using reversible logic. It is proved that the proposed multiplier architecture using the proposed TSG gate is better than the existing counterpart in literature in terms of reversible gates and garbage output.

III.UNSIGNED MULTIPLIER:

Unsigned multiplier can be used for designing reversible multiplier. Unsigned multiplier means the binary. It is defined as the if we assume binary representation the number is implicitly positive, there is value between 0 to255 and no other value. There is no sign, from logic test represent only the value of high bit and not the sign.

IV.WALLACE TREE MULTIPLER:

Reduction in number of partial products to be added can be achieved by using Wallace tree multiplier. Reduction in number of addition in critical path can be aimed using tree structure. Figure Below shows the architecture of 5 bit Wallace tree multiplie

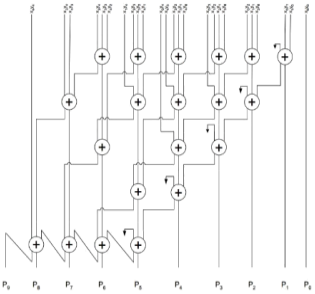


Fig1: Architecture of 5 bit wallace tree multiplier

V.SIMULATION RESULT

If A=0 and B=0 and C=0then output P=A ie.0and Q=B ie0 and C=Rie. AB xor Cie. output is 0 as shown in simulation result of reversible logic gate is shown in figure.

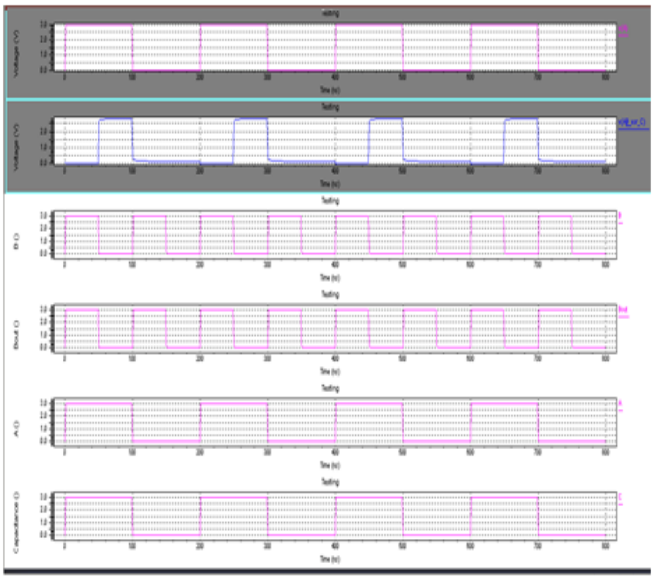


fig:Simulation of toffoli gate

FIGURE 2: Simulation result of Toffoli gate

Fig below shows the output of Feynman gatewhenA=0 then P=0 ie. A and Q=Axor Bie. 0.

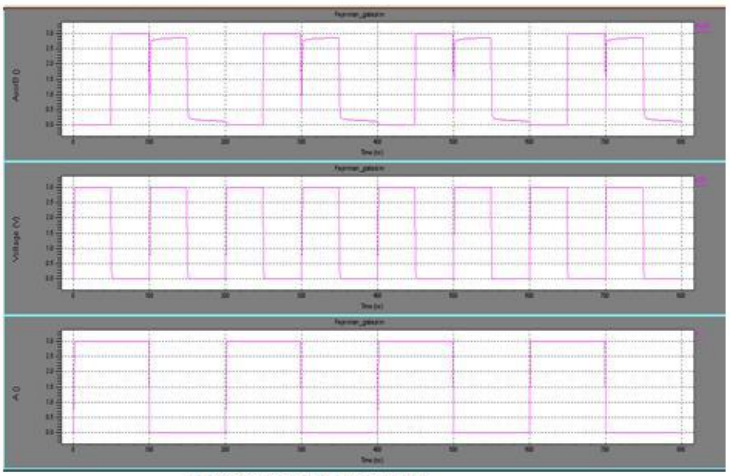


Fig:Simulation of feynman gate

FIGURE3:Simulation result of Feynman gate

VI.CONCLUSION

Wallace tree multiplier method reduces partial product array. And it can be used for implementation of reversible multiplier with the use of reversible logic gate using pass transistor logic. By using reversible logic gate the number of transistor is reduced and hence hardware complexity is less. Due to these reasons, Reversible multiplier is better and most favorable method than other methods. Implementation of reversible logic gate i. e. peres gate, HNG gate and tree multiplier. In this paper propose plan is design of peres gate, HNG gate and tree multiplier.

There are many uses of reversible logics such as low power CMOS, nanotechnology, quantum computing and optical computing.

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