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BASICS OF ENERGY-EFFICIENT DIGITAL DESIGN

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Abstract: Recent technological advancements have resulted in power being the major concern for digital system design. As device dimensions continue to decrease traditional constant field scaling can no longer be applied. The problem with this trend is that performance and power no longer scale proportionally leading to increasing power density. There are several other power issues. Energy efficiency has become main concern in the portable equipments to get better performance with less power dissipation. The less the power dissipation, the more efficient the circuit will be. This paper takes an overview of these power issues, need for energy efficient systems and discusses methodology for low-power digital system design.

Keywords: Efficiency, Power Dissipation, Consumption, Methodology.

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INTRODUCTION

The concern of power dissipation has been a part of design process since early 70s, but was less visible. Power dissipation has taken a back seat as a figure of merit, till early nineties. However at the end of the century, power dissipation has become the main design concern in many applications. The major challenge faced by digital system designers is to develop products which consume minimum power. Power saving must be achieved without compromising high performance and minimum area.

Energy and Power

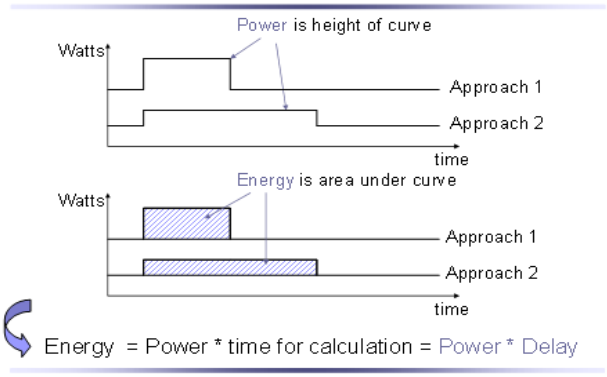

Fig. 1: Energy-power relation.

Energy and power are closely related. Power is measure of amplitude while energy is measure of span of area. Energy and power are related as-

Energy = Power * Delay

The power consumed by a circuit is defined as-

p(t) = i(t)v(t)

where, i(t) is the instantaneous current provided by the power supply, and v(t) is the instantaneous supply voltage.

Power minimization targets maximum instantaneous power or average power. The latter impacts battery lifetime and heat dissipation system cost, the former constrains power grid and power supply circuits design.

High power dissipation leads to:

- Reduced time of operation
- Higher weight (batteries)
- Reduced mobility
- High efforts of cooling
- Increasing operational cost
- Reduced reliability

CMOS is, by far, the most common technology used for manufacturing digital ICs. There are 3 major sources of power dissipation in a CMOS circuit:

$$\mathbf{P = P_{Switching} + P_{Short\text{-}Circuit} + P_{Leakage}}$$

$P_{Switching}$, called switching power, is due to charging and discharging capacitors driven by the circuit. $P_{Short\text{-}Circuit}$, called short-circuit power, is caused by the short circuit currents that arise when pairs of PMOS/NMOS transistors are conducting simultaneously. Finally, $P_{Leakage}$, called leakage power, originates from substrate injection and subthreshold effects. For older technologies, $P_{Switching}$ was predominant. For deep-submicron processes, $P_{Leakage}$ becomes more important.

Design for low-power implies the ability to reduce all three components of power consumption in CMOS circuits during the development of a low power electronic product. Optimizations can be achieved by facing the power problem from different perspectives: design and technology.

The dynamic energy consumption of CMOS circuitry is given by

$$\mathbf{P = \alpha C V^2 f}$$

Where α is switching activity, C is capacitive load, V is supply voltage and f is switching frequency.

The energy efficiency of a certain function is independent from the actual implementation, and thus independent from the issue whether an implementation is low power. It is possible to have two implementations of a certain function that are built with different building blocks, of

which one has a high energy efficiency, but dissipates more energy than the other implementation which has a lower energy efficiency, but is built with low-power components.

1. Need for low power designs

Recently power dissipation has emerged as important design goal beacause of following reasons:

- In battery powered portable systems, even if the energy density is more battery life is limited. Hence low power design techniques are essential for portable devices.
- Low power design is needed in high performance systems. With large integration density and improved speed of operation, systems with high clock frequency are emerging. This leads to focusing on optimizing systems for delay rather than energy.
- The power dissipation of the chip increases with increase in clock frequency. Since the dissipated heat must be removed effectively to keep the chip temperature at an acceptable level, the cost of packaging, cooling, and heat removal becomes a significant factor in these circuits.
- Another issue related to high power dissipation is reliability. As a result of high power dissipation, temperature of chip increases, leading to failure mechanisms like: silicon interconnect fatigue, package related failure, junction fatigue etc.
- As per the power budget, computers should not consume more than 5% of the total power consumption in a country. But 50% of office power is consumed by digital systems.

2. Power issues in digital systems:

- With the advent of CMOS technology, power density does not remain constant. Hence it is not possible to design solely for delay. Instead both energy and delay should be accounted for design process. The energy model can be combined with delay model to provide energy estimate for Logical effort.
- The difficult with energy-delay metrics is that these cannot be computed directly and cannot be used to achieve desired energy target or delay target.
- Energy and delay characteristics are related to physical dimensions of transistors.

- To be compatible with energy delay models, digital circuit sizing will only be allowed on an entire logic gate.

- System level approaches to power reduction do not offer into how the power saving is achieved. It is not known that a different realization may yield better results.

3. Low power design techniques

There can be multiple ways in which power reduction can be achieved in digital circuits. Few commonly used approaches are discussed here.

- Energy model: Energy model can be computed directly from gate size and output load. A basic energy model can be combined with RC-delay modeling to provide an energy estimate for logical effort(LE) delay optimized points. From these points the energy-delay space of digital circuits can be explored to identify the efficient region of operation and to identify energy-efficient characteristics of circuits.

- Despite having more stages than delay optimal, the energy still decreases. This is because by adding simpler gates to the output, the size of the complex gates in the circuit can decrease dramatically. Therefore, despite paying a slight delay penalty due to an extra logic stage, the energy of the design is decreased.

- There are essentially four ways to reduce power:

- Reduce the capacitive load *C*,

- Reduce the supply voltage *V*,

- Reduce the switching frequency *f*,

- Reduce the switching activity α.

- Adiabatic logic is an effective means for reducing power consumption. The term “adiabatic” is typically used to describe thermodynamic processes that have no energy exchange with the environment, and therefore, no energy loss in the form of dissipated heat. The electric charge transfer between the nodes of a circuit will be viewed as the process, and various techniques will be explored to minimize the energy loss, or heat dissipation, during charge transfer event. Fully adiabatic operation of a circuit is an ideal condition. In practical cases, energy dissipation associated with a charge transfer event is usually composed of an

adiabatic component and a non-adiabatic component. Therefore, reducing all energy loss to zero may not be possible, regardless of switching speed.

4. Low power design methodology

The methodologies which are used to achieve low power consumption in digital systems span a wide range, from process level to algorithm level. Device characteristics, device geometries and interconnect properties are significant factors in lowering the power consumption.

Circuit-level measures such as the proper choice of circuit design styles, reduction of voltage swing, and clocking strategies can be used to reduce power dissipation at transistor level. Architecture-level measures include smart power management of various system blocks, utilization of pipelining and parallelism, and design of bus structures. The power consumed by system can be reduced by proper selection of data processing algorithms, specifically to minimize the number of switching events for a given task.

In order to optimize the power dissipation of digital systems, low power methodology should be applied throughout the design process from system level to process level. Fig 2 shows different design levels of digital system.

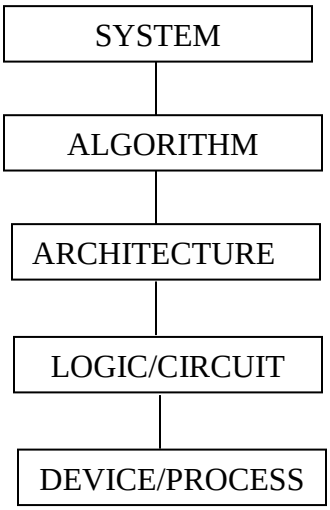

Fig. 2: Power reduction design space.

- **Power reduction through process technology**: One way o reduce power dissipation is to reduce power supply voltage. However delay increases significantly. To overcome this problem device should be scaled properly.

- **Power reduction through circuit/logic design:** To minimize power at circuit/logic level many techniques can be used:

- Use of static style over dynamic style.
- Reducing switching activity
- Optimize clock and bus
- Minimize device count and internal swing
- Reduce supply voltage and proper transistor sizing.
- Re-encoding sequential circuits.

- **Power reduction through architectural design:** At architectural level several approaches can be applied:

- Power management techniques where unused blocks are shutdown
- Low power architecture based on parallelism, pipelining etc
- Memory partition with selective enable.
- Reduction of no. of global buses.
- Minimization of instruction set

- **Power reduction through Algorithm selection:** The techniques at algorithm level are:

- Minimizing no of operations and hence no. of hardware resources.
- Data coding for minimum switching activity.

- **Power reduction in system integration:** System level is important to whole process of power optimization. Some techniques are:

- Utilize low system clock
- High level of integration. Integrate off-chip memories.

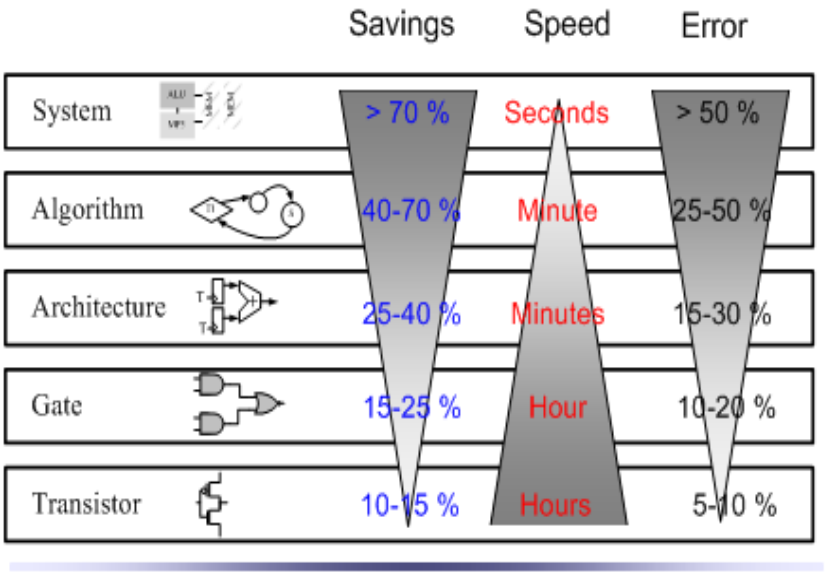

Fig. 3: Levels of optimization.

CONCLUSION

Digital design aims at striking a balance between performance and power efficiency. Designing low-power applications is a multi-faceted problem, because of large number of system specifications and the variety of degrees of freedom that designers have to cope with power reduction. Power minimization is often a process of adjusting parameters in various trade-offs. Despite the differences in optimization and trade-off possibilities at the various levels of abstraction, the common themes of the low-power techniques are quite similar.

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