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INDUCTION MOTOR DRIVE WITH SINGLE DC LINK TO MINIMIZE ZERO SEQUENCE CURRENT IN INVERTER TOPOLOGY

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Abstract: A multilevel inverter topology for a four-pole induction-motor drive is proposed in this paper, which is constructed using the stator winding arrangement of induction-motor. A single dc source with a less magnitude when compared with conventional five-level inverter topologies is used in this topology. Therefore, power balancing issues (which are major challenges in conventional multilevel inverters) are minimized. As this configuration uses a single dc source, it provides a path for zero-sequence currents because of the zero-sequence voltages present in the output, which will flow through the motor phase winding and power electronic switches. To minimize these zero-sequence currents, sine–triangle pulse width modulation (SPWM) is used, which will shift the lower order harmonics near to switching frequency in the linear modulation region. However, in the case of over modulation, harmonic voltages will be introduced close to the fundamental frequency. In this regard, a modified SPWM technique is proposed in this paper to operate the drive in the over modulation region up to the modulation index.

Keywords: Induction-motor drive, modified sine-triangle pulse width modulation, multilevel inverter, over modulation.

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INTRODUCTION

Multilevel inverter technology has been widely used for the control of medium and high voltage ac drives applications because of its improved output voltage quality, better harmonic performance, less voltage stress on power electronic devices. The basic concept of the multilevel inverter is to achieve the staircase voltage waveform by using more low rated power electronic switches and voltage sources[1]. In case of conventional multilevel inverters the number of output voltage levels increases the requirement of series connected switches. The improvement, availability, reliability and the power segmentation of the speed drive application became an essential purpose for the industrialization of the high power equipment. To obtain a quality output voltage or a current waveform with a minimum amount of ripple content, they require high-switching frequency along with various pulse-width modulation (PWM) strategies.

The semiconductor switching devices should be used in such a manner as to avoid problems associated with their series parallel combinations. The basic concept of multilevel inverters is to achieve the staircase voltage waveform by using more low-rated power electronic switches and voltage sources. As the number of output voltage levels increase, the requirement of series-connected switches will also increase in the case of conventional multilevel inverters such as diode-clamped and flying-capacitor (FC) multilevel inverters. Therefore, if any of the switches fails, the entire topology has to be shut down [5], resulting in decreased system reliability. The multilevel inverter includes an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The action of the power semiconductors is represented by an ideal switch induction motor drive by using four conventional two-level inverters only, with the advantage of two identical voltages profile winding coils of four pole induction motor. The identical voltage profile winding coils are disconnected and each part of the winding is fed with two two-level inverters from both sides. Inverters are fed with single DC link with less magnitude. The proposed topology uses sine-triangle PWM to generate the pulses for the switches of each inverter which will also minimize the common mode currents circulating in the motor phase windings because of the common DC link. A multilevel inverter topology for four pole induction motor drive is constructed using induction motor stator winding arrangements. A single dc source minimizes power balancing issues and provides a path for zero sequence currents. A single dc source with less magnitude will be used. Thus a single dc source provides a path for zero sequence currents. The zero sequence currents will be minimized by using sine-triangle pulse width modulation technique. Objective of the proposed work is to design an induction motor drive with single dc link to minimize zero sequence current in inverter topology. The reliability will be increased

using H-bridge configuration. Sine-triangle pulse width modulation scheme will be effective only in linear modulation. For over modulation region modified SPWM technique will be used.

II. LITERATURE REVIEW

Multilevel inverter topology has emerged as an important alternative in the area of high power high voltage energy control. There is some research work and literatures are as given below:

K. Kumar (2015) proposed a quad two-level inverter configuration for four-pole induction motor drive with single DC link. In this paper a single dc source is compared with conventional five-level inverter topology. Power balancing issues are minimized. Sine-triangle pulse width modulation is used to minimize zero-sequence currents[1]. T. Boller (2014) proposes neutral point potential balancing using synchronous optimal pulse width modulation of multilevel inverters in medium voltage high power AC drives. This paper presents neutral point potential balancing by maintaining low harmonic distortion. The method is applicable for four-level inverters or higher[2]. A. Somani (2013) proposes the causes of circulating currents in PWM drives with open-end winding AC machines. Electric drives with open-end winding ac winding has certain advantages over drives with star-or-delta connected machines[3]. A. Edpuganti (2014) proposes new optimal pulse width modulation for single DC-link dual inverter fed open-end stator winding induction motor drives. In medium voltage high power drives for improving the overall efficiency of drive system low device switching frequencies are preferred[4]. N. Bodo (2013) presents carrier-based PWM technique for a five-phase open-end winding drive topology. In conjuction with a multiphase open-end winding drive topology, there is a implementation of level-shifted and phase-shifted carrier-based modulation methods[5]. M. A. Parker (2013) proposes a distributed control of a fault-tolerant modular multilevel inverter for direct-drive wind turbine grid interfacing. To achieve a fault tolerance and high reliability for wind turbines a modular generator and converter topologies are used [6]. J. Ewanchuk and J. Salmon (2013) proposed a method for supply voltage boosting in an open-ended induction machine using a dual inverter system with a floating capacitor bridge. In this paper an operational approach to an induction machine is presented which uses an open end winding connected to dual inverter system[7]. J. Ewanchuk (2013) proposed a three-limb coupled inductor operation for paralled multi-level three-phase voltage sourced inverters. In high current applications, parallel connected three-phase voltage source inverter represents a modular solution to improve the system power conversion quality[8]. Milan Darijevic, Martin Jones (2015)proposed an open-end winding four-level five-phase drive. The topology gives advantages of a modular structure with fewer semiconductor component and has a greater potential for fault tolerance[9]. A. Dey (2013) proposed a space vector-based hysteresis current

controller for a general n-level inverter-fed drive with nearly constant switching frequency control. Controller is implemented on a five-level VSI fed 7.5 KW induction motor drive[10].

III. PROPOSED MULTILEVEL INVERTER TOPOLOGY

The five-level inverter topology presented uses three dc sources to obtain a five-level voltage waveform. Mostly diode bridge rectifiers are used for providing dc supply. Therefore, in regenerative braking, it requires three braking rheostats and three control mechanisms to protect the rectifier units, which complicate control and power circuits. The two disconnected IVPWCs are supplied with four conventional two-level inverters, and all of them are connected to the same dc source.

The maximum voltage blocking capacity of all two-level inverter switches is equal to input dc source voltage (vdc/4). Two switches in the same leg of the two-level inverters complement each other. The switches used are bidirectional (four-quadrant) switches that can allow the current in both directions and can block the voltage in both directions. The maximum voltage blocking capacity of these switches is vdc/8 only. All these (main and auxiliary) switches are switched in such a way that it produces five-level voltage ((vdc/2), (vdc/4), 0, (−vdc/4), (−vdc/2)) across the motor phase winding. Permanent shorting of the bidirectional switches cause unequal voltages across IVPWCs (Identical voltage profile winding coil), during some ((−vdc/4), 0, (vdc/4)) voltage-level synthesis. Hence, control of these bidirectional switches is important. The proposed topology is free from neutral-point voltage balancing issues because the clamping diodes are not used unlike in the diode-clamped topologies. The capacitor voltage balancing issues are also eliminated because it does not require any capacitor banks unlike FC inverters. Only a single dc source is used in this configuration; therefore, power balancing issues and issues in regenerating mode are minimized. The magnitude of the dc bus requirement is also less (vdc/4). The only additional requirement in this topology is six bidirectional switches with voltage rating of vdc/8. Gating pulses for the proposed multilevel inverter are generated using SPWM. Multilevel inverter (MLI) cascade inverter with diodes blocking the source is used in this topology. It works in two modulation region linear modulation region and over-modulation region. This inverter was later derived into the Diode Clamped Multilevel Inverter; also called Neutral-Point Clamped Inverter (NPC). In NPCMLI topology the use of voltage clamping diodes is essential. A common DC-bus is divided by an even number, depending on the number of voltage levels in the inverter, of bulk capacitors in series with a neutral point in the middle of the line. Similar topology to the NPCMLI topology is the Capacitor Clamped (CC), or Flying Capacitor, multilevel inverter topology.

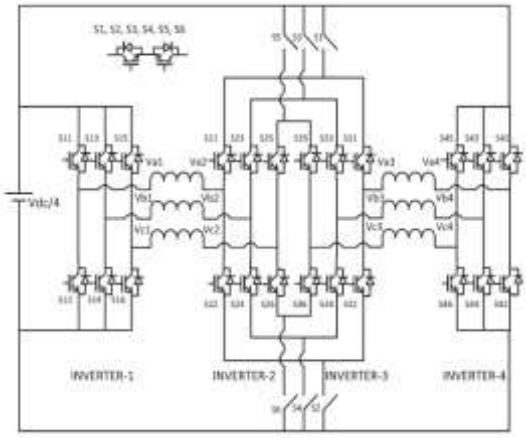
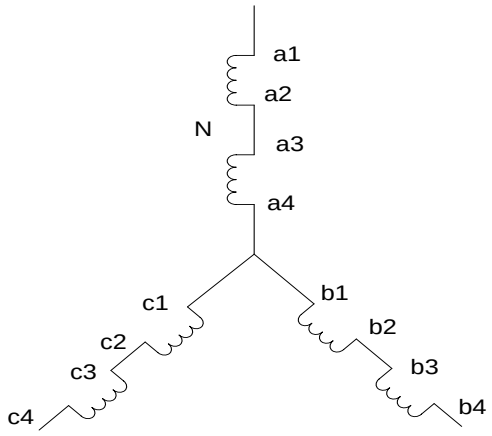


Figure 1: Proposed multilevel inverter topology.
Source - IEEE Transaction on Industrial Electronics January 2015

Instead of using clamping diodes it uses capacitors to hold the voltages to the desired values. As for the NPCMLI switch-diode valve pairs are used. Instead of using clamping diodes one or more capacitors are used to create the output voltages. They are connected to the midpoints of two valve pairs on the same position.



(a)

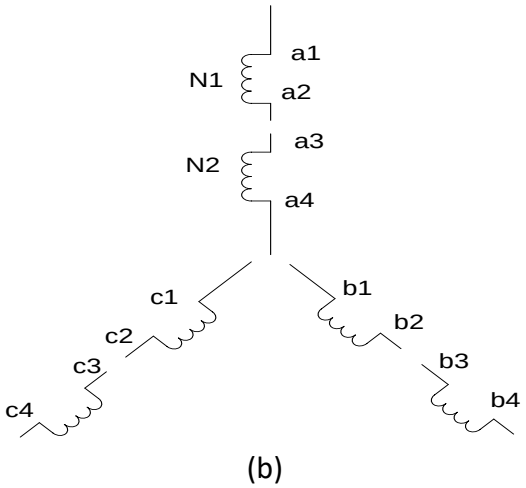


Figure 2: Induction motor stator winding. (a). General arrangement.
(b). Arrangement for the proposed inverter.
Source - IEEE Transaction on Industrial Electronics January 2015

The above figure.2 (a) shows conventional four-pole induction motor with two windings connected in series. Figure.2 (b) shows conventional four-pole induction motor with two disconnected winding. The two windings are disconnected such that both have equal number of turns. When it comes to multilevel inverter modulation there are basically two groups of methods: modulation with fundamental switching frequency or high switching frequency PWM. For both cases a stepped output waveform is achieved, but with the high switching frequency methods the steppes are modulated with some sort of PWM. Independent of switching frequency choice there are, however, also space vector methods use. Multilevel PWM methods uses high switching frequency carrier waves in comparison to the reference waves to generate a sinusoidal output wave, much like in the two-level PWM case. To reduce harmonic distortions in the output signal phase-shifting techniques are used. PWM technique is extensively used for eliminating harmful low-order harmonics in inverters. In PWM control, the inverter switches are turned ON and OFF several times during a half cycle and output voltage is controlled by varying the pulse width. SPWM techniques are characterized by constant amplitude pulses with different duty cycle for each period. On the other hand, an open-end winding induction motor supplied by SVPWM-controlled multilevel inverters with a single dc source will provide path for the zero-sequence currents because of the dominant lower order harmonic voltages in the inverter output voltage. A five-level inverter topology for a four-pole induction-motor drive with a single dc link is presented in, which has used SPWM to minimize the zero-sequence currents though the motor phase windings. However, this scheme is effective in the linear

modulation only. In this paper, a modified SPWM technique is proposed to operate the five-level inverter configuration (using quad two level inverters) also in over modulation region. It is well known that, in a conventional ac machine, the winding coils which are 360◦ (electrical) apart will have identical voltage profiles across them. Thus, the four-pole induction motor consists of two IVPWCs (where the number of IVPWCs is equal to the number of pole pairs). In the conventional four-pole induction motor, these two windings are connected in series. However, in this paper, these are disconnected. As the two windings are disconnected exactly with an equal number of turns. After disconnection of two windings waveforms of both are compared and studied. Zero sequence currents are minimized after disconnection.

CONCLUSION

Multilevel voltage source converters are emerging as a new breed of power converter options for high-power applications. In this paper an optimized five-level inverter topology is presented for a four pole induction motor drive. This topology has developed by using the advantage of two identical voltage profile winding coils per phase in a four pole induction motor. The identical voltage profile winding coils are disconnected and each part of the winding is fed with two two-level inverters from both sides minimizing the power balancing issues. The magnitude of dc source voltage requirement is also very less compared with that of conventional five-level inverter topologies. This will increase the reliability of the system during fault condition when compared with conventional neutral point capacitor or Flying capacitor topologies. Thereby four two-level inverters are required to generate five voltage levels. All two-level inverters are fed with single DC link with the magnitude Vdc/4. Zero sequence currents will be minimized by using single dc link. This topology is simulated using MATLAB Simulink. The waveforms of induction motor are observe and studied.

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