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DC-DC CONVERTER FOR INTEGRATION OF SOURCES

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Abstract: This paper presents a multilevel with separate dc sources and solar dc source balancing the power with SPWM technique. The deals simulation and hardware design of single phase multi-level inverter with separate two dc sources using conventional method and multicarrier pulse width modulation technique and the output results of both methods are compared and multilevel inverter is designed. Multilevel inverters include an arrangement of semiconductors and dc voltage sources required to generate a stepped output voltage waveform. The number of input DC voltages depends on the number of inverter output voltage levels and as the levels are increased the harmonics are reduced.

Key Words: 5-level inverter, PV Cell, DC supply, SPWM Technique, THD.

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INTRODUCTION

The multilevel concept is used to decrease the harmonic distortion in the output waveform without decreasing the inverter power output. This project presents the most important topologies like diode-clamped inverter (neutral- point clamped), capacitor-clamped (flying capacitor), and cascaded multilevel with separate dc sources and solar dc source balancing the power with SPWM technique. The deals simulation and hardware design of single phase multi level inverter with separate two dc sources using conventional method and multicarrier pulse width modulation technique and the output results of both methods are compared and multilevel inverter is designed. Multilevel inverters include an arrangement of semiconductors and dc voltage sources required to generate a stepped output voltage waveform. The number of input DC voltages depends on the number of inverter output voltage levels and as the levels are increased the harmonics are reduced. Pulse width modulation is the main control strategy implemented in the power electronics. This is the best way of driving modern power electronic devices. Most of the power electronic circuits are controlled by PWM signals of various forms such as multi carrier PWM. Multilevel inverter structures are becoming increasingly popular for high power applications, their switched output voltage harmonics can be reduced since semiconductors are connected in series for multilevel inverter structures the number of levels increases, the synthesized output waveform has more steps, producing a very fine stair case wave and approaching very closely to the desired sine wave. It can be easily understood that as motor steps are included in the waveform the harmonic distortion of the output wave decrease, approaching zero as the number of levels approaches infinity.

II. LITERATURE REVIEW

Multilevel inverter of new approach with two sources is the latest area of interest amongst the power electronic researchers. Some of the research work and literature work are given below.

Naresh Kumar Varathe, Ketan Mishra, Shubham Shivhare (2014) proposes that inverter is used for maximum control techniques of output voltage and current. That power semiconductor device able to reduces the harmonics and provide the high o/p voltage. Result is compared with the conventional single phase seven level inverter grid connected PV inverter. THD and EMI result also in this paper with reduce the losses [1]. Nurul Aisyah Yusof, Norazliani Md Sapari, Hazlie Mokhlis, Jeyraj Selvaraj (2012) proposed that Power electronic converters were developed for integrating the photovoltaic (PV) arrays and utility grid. Inverters are needed to

convert the direct current electricity produced by the PV array into alternating current electricity required for loads [2].

Kapil Jain, Pradyumn Chaturvedi (2012) suggested the elementary concept of multilevel converter to achieve higher power to use a series of power semiconductor switches with several lower voltage dc source to perform the power conversion by synthesizing a staircase voltage waveform [3].

Nasrudin A. Rahim, Krismadinata Chaniago, JeyrajSelvaraj (2011) proposed that a novel power conversion structure for grid-connected photovoltaic applications is presented [4].

Divya Subramanian, Rebiya Rasheed (2013) suggested that multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages [5].

K.Surya Suresh and M.Vishnu Prasad investigates the performance of a PV cell connected Multi Level Inverter topology. These MLI's are suitable in high voltage & high power application due to their ability to synthesize waveforms with better harmonic spectrum. The MCPWM Cascaded Multilevel inverter strategy enhances the fundamental output voltage and reduced Total harmonic distortion [6]. Thanuj kumar jala and G. Srinivasa rao (2012) suggested that a single-phase sevenlevel inverter for grid-connected photovoltaic systems, with a novel pulse width-modulated (PWM) control scheme. Three reference signals that are identical to each other with an offset that is equivalent to the amplitude of the triangular carrier signal were used to generate the PWM signals [7]. Chetanya Gupta, Devbrat Kuanr, Abhishek Varshney, Tahir Khurshaid, Kapil Dev Singh (2014) the effectiveness of the proposed strategy in terms of computational efficiency as well as the capability of the inverter to produce very low distorted voltage with low-switching losses. This research aims to extend the knowledge about the performance of different clamped multilevel inverter through harmonic analysis [8].

Loganathan., Prabhakaran, Indhumathy (2015) proposed that the solar fed cascaded multilevel inverter produces AC output voltage of desired magnitude and frequency. Since the inverter is used in a PV system, a optimization technique is used to obtain the switching angles to reduce the harmonic content [9]. Neelashetty Kashappa, Ramesh Reddy (2012) in the proposed scheme, control circuit is designed using 89C51 microcontroller to produce sinusoidal pulse width modulation(SPWM).The developed system can be operated at very high modulation frequencies of upto 200 KHz producing sustained output [10].

III. THEORY

Several multilevel topologies:-

1] Multilevel Diode Clamped/Neutral Point Inverter

Multilevel inverter (MLI) cascade inverter (cascaded inverters will be presented in a later chapter) with diodes blocking the source. This inverter was later derived into the Diode Clamped Multilevel Inverter; also called Neutral-Point Clamped Inverter (NPC) the NPCMLI topology the use of voltage clamping diodes is essential. A common DC-bus is divided by an even number, depending on the number of voltage levels in the inverter, of bulk capacitors in series with a neutral point in the middle of the line.

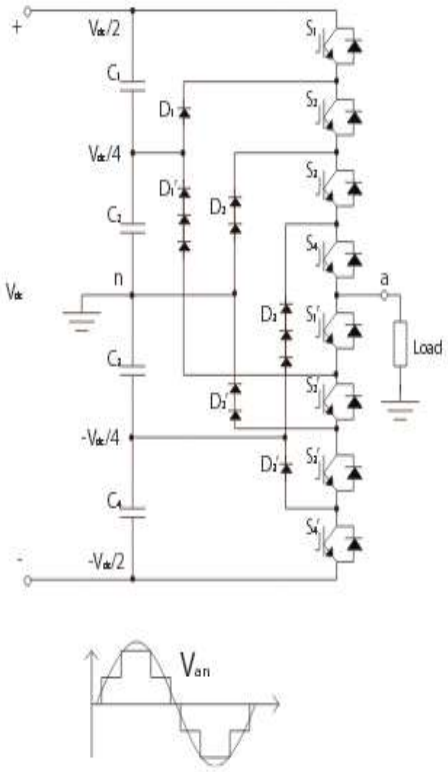

Fig.1 One phase-leg for a two-level NPC Inverter

Diode clamped multilevel inverters use clamping diodes in order to limit the voltage stress of power devices. It was first proposed in 1981 by Nabae, Takashi and Akagi and it is also known as neutral point converter. A *k* level diode clamped inverter needs (2*k* – 2) switching devices, (k – 1) input voltage source and (k – 1) (k – 2) diodes in order to operate. *Vdc* is the voltage present across each diode and the switch.

Advantages of Diode Clamped Multilevel Inverters

- Capacitance of the capacitors used is low.

- Back to back inverters can be used.
- Capacitors are pre charged.
- At fundamental frequency, efficiency is high.

Applications of Diode Clamped Multilevel Inverters

- It is used when a high voltage Dc and Ac transmission lines are interfaced.
- For variable speed control of high power drives.
- Static variable compensation.

2] Multilevel Capacitor Clamped/Flying Capacitor Inverter, CCMLI

3] Cascaded Multicell Inverter, CMC

4] Generalized P2-cell Multilevel Inverter, GML

5] Reversing Voltage Multilevel Inverter, RVMLI

6] Modular Multilevel Inverter, M2I

7] Generalized Multilevel Current Source Inverter, GMCS

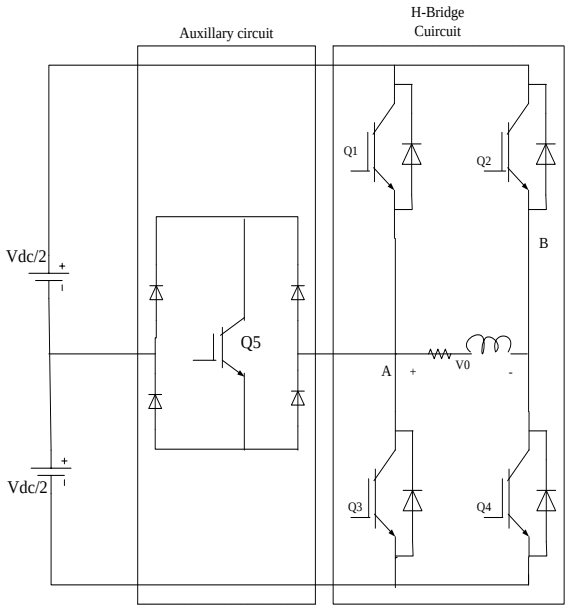

Figure 2. Topology of 5-level multilevel inverter.

TABLE I. THE SWITCHES ON-OFF CONDITION FOR 5- LEVEL MULTILEVEL INVERTER

Output Voltage	Q1	Q2	Q3	Q4	Q5
+Vdc	1	0	0	0	1
+Vdc/2	0	0	0	1	1
0	0	0	1	1	0
-Vdc	0	1	0	0	1
-Vdc/2	1	0	0	1	0

Note: “1” for ON. “0” for OFF

III. MODULATION TECHNIQUE

A. PWM Modulation Technique for 5-level Multilevel Inverter

The modulation technique used in this inverter topology is sinusoidal pulse width modulation (SPWM) technique. The principle is to generate gate signal by comparing a triangular carrier signal with two reference (sinusoidal) signals, which having same frequency and in phase, but different offset voltages as shown in Figure 1[2].

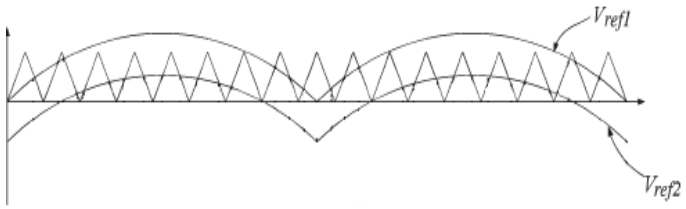

Figure 3. PWM switching signal generation for 5-level multilevel inverter.

According to the amplitude of the voltage reference, V*ref*, the operational interval of each mode varies within a certain period. The modes are separated as

Mode 1: $0 < \omega t \leq \theta_1 \& \theta_2 < \omega t \leq \pi$
Mode 2: $\theta_1 < \omega t \leq \theta_2$
Mode 3: $\pi < \omega t \leq \theta_3 \& \theta_4 < \omega t \leq 2\pi$
Mode 4: $\theta_3 < \omega t \leq \theta_4$

The phase depends on the modulation index. The modulation index of the proposed five-level PWM inverter is defined as

$$M=\frac{Am}{2Ac}$$

Where AM is the peak value of reference voltage and AC is the peak value of carrier wave.

IV. Real Time Hardware Implantation been Tested in Simulation

The general block diagram of a multilevel inverter fed by pulse generator is shown in Figure. The ac supply is fed to rectifier which converts alternating current (AC) and additional source of solar for bleaching. The dc supply sends the gate pulses to the driver circuit through pulse generator. The battery source is fed to cascaded multilevel inverter and load and various preface result analyzing.

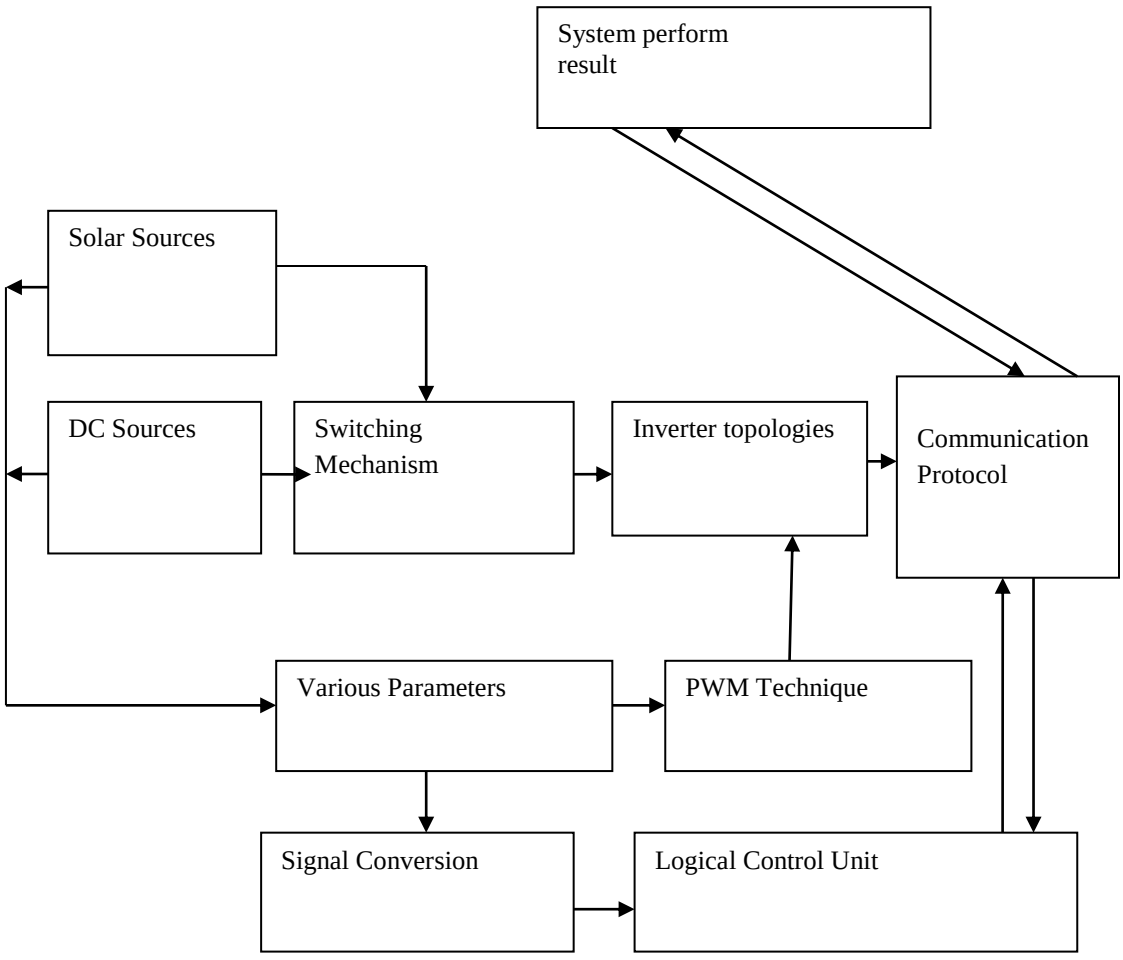

Fig.4 Simple hardware construction diagram

V. FFT ANALYSIS FOR THD

- The harmonics distortion principally comes from

Nonlinear-Type Loads.

- The application of power electronics is causing increased level of harmonics due to switching.
- Harmonic distortion can cause serious failure/damage problem.
- Harmonics are important aspect of power operation that requires Mitigation.
- Over-Sizing and power filtering methods are commonly used to limit overheating effects of sustained harmonics.

VI.CONCLUSION

The use of multilevel inverter in PV system was accepted in power system since it gave a lot of advantages. More number of levels of multilevel inverter will give better performance in the system. In this paper, from the simulations and the results, 5-level multilevel inverter had given more efficient performance in terms of the power factor, THD and its efficiency. It also is more suitable for the purpose of integrating PV arrays and grid system. By controlling the modulation index, the desired number of level of the inverter output voltage can be achieved. Multilevel inverter offers improved output voltage and lower THD. It is also more suitable for the purpose of integrating PV arrays and grid system.

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REFERENCES

1. Naresh Kumar Varathe, Ketan Mishra, Shubham Shivare, “Simulation and Analysis of Single Phase Seven Level Inveter with Number of Switches are Reduce” International Journal of Emerging Trends & Technology in Computer Science (IJETTCS) Volume 3,Issue 3 May-June 2014.
2. Nurul Aisyah Yusof, Norazliani Md Saparil, Hazlie Mokhlis, Jeyraj Selvaraj “A Comparative Study of 5-level and 7-level Multilevel Inverter Connected to the Grid” 2012 IEEE International Conference on Power and Energy (PECon), Kota Kinabalu Sabah, Malaysia 2-5 December 2012.

3. Kapil Jain,Pradyumn Chaturdevi "Matlab-based Simulation & Analysis of Three-level SPWM Inveter" International Journal of Soft Computing and Engineering (IJSCE) ISSN: 2231-2307, Volume-2, Issue-1, March 2012.
4. Nasrudin A. Rahim, Krismadinata Chaniago, Jeyraj Selvara "Single Phase Seven Level Grid Connected Inverter for Photovoltaic System" IEEE Transaction on photovoltaic Industrial Electronics, VOL-58, No.6, JUNE 2011.
5. Divya Subramanian, Rebiya Rasheed, "Five Level Cascaded H-Bridge Multilevel Inverter Using Multicarrier Pulse Width Modulation Technique" International Journal of Engineering and Innovative Technology (IJEIT) Volume 3, Issue 1, July 2013.
6. K.Surya Suresh and M.Vishnu Prasad "PV Cell Based Five Level Inverter Using Multicarrier PWM" International Journal of Modern Engineering Research (IJMER) Vol. 1, Issue 2,March-April 2013,pp. 545-551 ISSN: 2249-6645.
7. Thanuj Kumar Jala and G.Srinivasa rao "A Novel Nine Level Grid Connected Inverter for Photovoltaic System" IJMER VOl.2, Issue 2, pp 154-459, March-April 2012.
8. Chetanya Gupta, Devbrat Kuanr, Abhishek Varshney, Tahir Khurshaid, Kapil Dev Singh "Harmonic Analysis of Seven and Nine Level Cascaded Multilevel Inverter Using Multicarrier PWM Technique" International Journal of Power Electronics and Drive System (IJPEDS) Vol. 5,No.1, July 2014, pp. 76-82 ISSN:2088-8694.
9. Logananthan. G1, Prabhakaran B2, Indhumathy K3 Harmonic Elimination in Solar Fed Cascaded Multilevel Inverter Using Optimization Techniques" International Journal of Innovative Research in Science, Engineering and Technology ISO 3297:2007 Certified Organization Volume 4,Special Issue 2, February 2015.
10. Neelashetty Kashappa, Ramesh Reddy Implementation of a low cost PWM Voltage Source Multilevel Inverter International Journal of Engineering and Technology, Volume 2, No. 2, February 2012.