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A REVIEW ON: DESIGN OF 32-BIT MAC UNIT FOR COMPLEX NUMBERS IN VHDL

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Abstract: Dadda multiplier has been used in the MAC unit and comparison is done based on the power, speed and area. Four 32 bit Dadda multiplier, 64 bit CLA and the complex multiplier are used. This proposed method is to achieve low propagation delay, resource utilization and to increase the speed of processor. The high speed implementation of such a multiplier has wide range of application in image processing, arithmetic logic unit and VLSI signal processing.

Keywords: Carry look ahead adder, complex number arithmetic, multiply accumulate circuit, DADDA multipler

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INTRODUCTION

The multiply-accumulate operation is common step that compute the product of two numbers and add that product to an accumulator . The Hardware unit that performs the operation is known as Multiply Accumulate (MAC). With the increasing popularity of the smart phones and TABs, speed of the processor has become so important nowadays. The need for the processor's speed is more exploited for gaming and multimedia application purposes, it can also be arranged in fields like medical for faster diagnosis, in automation industry for higher throughput and so on. Since most of the signal processing operations is done by adders and multipliers units, efficient design of these units increases the speed of the processor. MAC unit is mainly used in several multimedia applications, careful design of this MAC unit leads to the design of high performance processor. The speed of the conventional MAC unit is optimized by using various frontline multipliers like Wallace tree multiplier, Booth Multiplier, Baugh-Wooley multiplier.

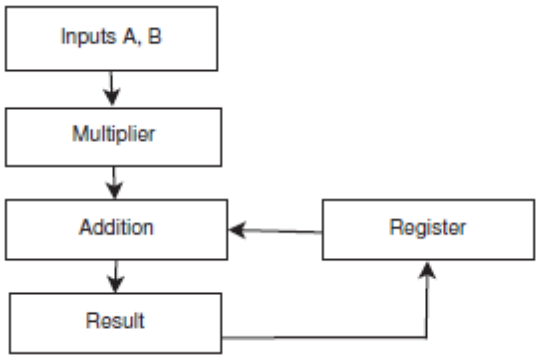


Fig 1: Block Diagram of MAC

The MAC operation modifies an accumulator:

$$a \leftarrow a + (b \times c)$$

The digital signal processors are used to perform the digital signal processing operations like convolution, correlation, transform and filtering. All the above mentioned digital signal processing operations are in the form of multiplication and repeated addition. So multiply accumulate circuit (MAC) is the heart of the digital signal processor. The signal sequences can be represented as fixed/floating point complex numbers. Complex numbers are playing a vital role in electronics and digital signal processing (DSP), because they are easy way to represent and manipulate the most useful real world sinusoidal waveforms. The basic blocks of MAC is

shown in Fig. 1, where the inputs A and B are multiplied then the multiplication result is added with the previous MAC result. If A, B are n bits wide then the multiplication result will be 2n bits wide. Array multiplier and Wallace tree multiplier are the popular multipliers that are used in hardware implementation. The Wallace tree multiplier has the time complexity as O(log2 n). The array multiplier can be further classified into two categories namely, ripple carry array multiplier and carry save array multiplier. The conventional fixed point complex number multiplier-cum-accumulator is shown in Fig. 2, where four fixed point multipliers and four fixed point adders are used. In the architecture two fixed point multiplier-cum accumulators, two fixed point multipliers and two fixed point adders are involved.

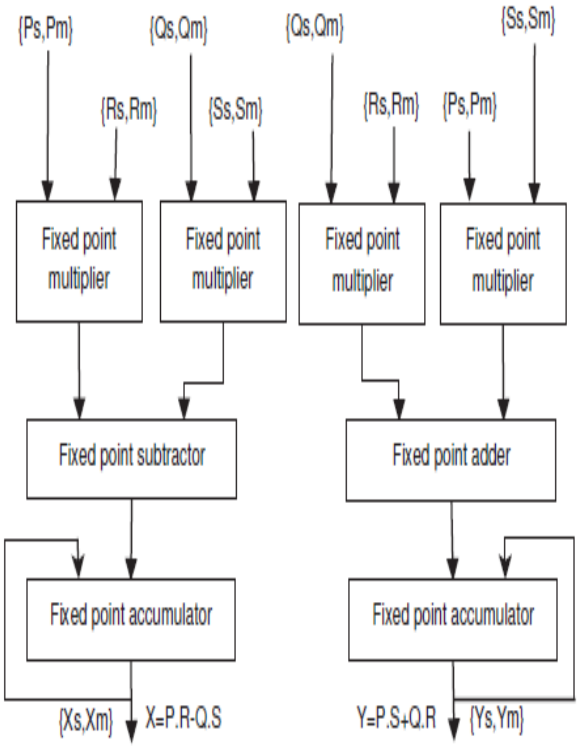


Fig 2: Complex Multiplier

REVIEW

Rahul Narasimhan. A, R. Siva Subramanian has developed an optimized co-processor unit, designed specifically for executing the DSP application is proposed. It can be used as a co-processor for the ACORN ARM processor. The co-processor comprises of one MAC unit, control unit, a 32 bit output registers and register files for storing the input values and other co-

efficient. The co-processor is designed to execute a FIR filter. Vedic multiplier and booth multiplier has been used in the MAC unit and comparison is done based on the power, speed and area.[1]

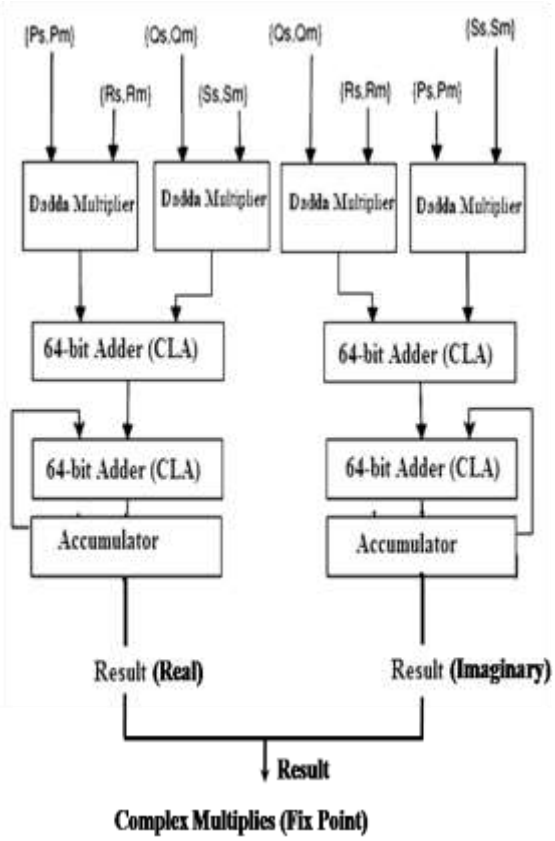
RamandeepKaur , Rahul Malhotra , Sujay Deb has developed this paper proposes an FIR (Finite Impulse Response) filter based on Multiply-Accumulator (MAC) Unit to suppress the PLI noise. The performance of this filter largely depends on the speed and power of the MAC unit employed inside the filter. The current work compares various MAC units on Power, Performance and Area (PPA) benchmarks. It is shown that Booth-Wallace-Carry Look Ahead adder (CLA) based MAC is optimised for both timing and power which shows 6.2% improvement in performance and 12.1% reduction in power from other implemented designs. The convergence time of the algorithm is observed to be less than 0.2 &sec with significant power savings to improve battery life. [2]

Mohamed AsanBasiri M, Noor MahammadSk has developed a high performance 32-bit radix-2 fixed point complex number MAC is proposed, where the real and imaginary parts can be computed by sending the previous MAC result. The experimental results are showing the proposed fixed point complex number MAC is giving better performance than the conventional fixed point complex number MAC. The proposed architecture achieves an improvement factor of 32.4% in Wallace tree and 19.1% in Braun multiplier based fixed point complex number MAC with out pipeline using 45 nm technology library. The same architecture achieves an improvement factor of 14.6% in Wallace tree and 12.2% in Braun multiplier based fixed point complex number MAC with pipeline.[3]

MarojuSaikumar , D.Ashok Kumar , Dr.P.Samundiswary has developed MAC unit model is designed by including the various multipliers such as Array Multiplier, Ripple Carry Array Multiplier with Row Bypassing Technique, Wallace Tree Multiplier and DADDA Multiplier in the multiplier module and the performance of MAC unit models is analyzed in terms of area, delay and power. The performance analysis of MAC unit models is done by designing the models in Verilog HDL. Further, this work can be extended by designing of MAC unit with higher number of bit sizes such as 16, 32 and 64 and also for designing applications like ALU, filters etc. [4]

PROPOSED METHODOLOGY:

In proposed methodology, designing of all 32-bit Dadda multiplier , 64-bit carry look ahead adder and the complex multiplier , And then after work in these project VHDL implementation of complex multiplier. Then comparison of result with available literature.



Complex Multiplies (Fix Point)

CONCLUSION

In this paper we are comparing the result of conventional MAC and Proposed MAC, a high performance 32-bit fixed point complex number MAC is proposed , where the real and imaginary parts can be computed. The proposed fixed point complex number MAC is giving better performance than the conventional fixed point complex number MAC.

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