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EFFECTIVE IMPLEMENTATION OF INTERPOLATOR AND DECIMATOR USING FPGA

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Abstract- The purpose of this paper is to implement interpolators and decimators on Field Programmable Gate Array (FPGA). In VHDL interpolators and decimators of different word lengths (WL) are implemented. An FIR filter is designed in such a way that it can be implemented for different word lengths (8-bit, 12-bit, 16-bit). Today's advance FPGA devices and high speed digital to analog converters make it possible to use advanced direct synthesis technologies in professional equipment and this is cost-sensitive, that's why effective usage of available hardware resources is important in advance technology. For every electronic device, lower circuit complexity is always an important design as it reduces the cost. There are many uses where the sampling rate must be changed. Interpolators and decimators are use to increase or decrease the sampling rate. In multi rate DSP systems up-sampler and down sampler are used to change the sampling rate of digital signal.

Keywords: FIR filters; FPGA; VHDL; INTERPOLATOR; DECIMATOR

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INTRODUCTION

Nowadays, the advance digital systems are more complex. They consist of several DSP (Digital Signal Processing) processors that works at different sampling frequencies. A common sampling rate should be employed for these signals to mix the signals digitally. In-order to match the higher sample rate signal the stream at lower sample rate is interpolated to increase the sample rate. Interpolators can be found in mixed-signal processing systems, digital receivers and in sigma-delta modulators. Decimators are used to reduce the higher sample rate to lower sample rate. In the area of digital signal processing, the use of digital representation of signals for transmission and storage has created challenges. The applications of digital FIR filter and up/down sampling techniques are found everywhere in modem electronic products.

II. LITERATURE REVIEW

1. Rajesh Mehra and Shaily Verma described FPGA Based Design of Direct Form FIR Polyphase Interpolator for Wireless Communication. International Journal of Electrical Electronics &Telecommunication Engineering, ISSN:2051-3240, Vol.44,Issue.1 1108
2. Abdelhakim SAHOUR and Mohamed Benouaret designed FPGA Implementation of Daubeshies Polyphase-Decimator filter. International Journal of Computer Applications (0975 – 8887) Volume 7– No.10, October 2010
3. Dr. K. Babulu, Mohammad shaffi studied FPGA Implementation of Multi-Rate Reconfigurable
Architecture with low complexity FIR Filters. International Journal of Emerging Technology and Advanced Engineering Website: www.ijetae.com (ISSN 2250-2459, Volume 2, Issue 10, September 2012)
4. V. Jayaprakasan1, M. Madheswaran described FPGA Implementation of FIR based Decimation
Filter Structure for WiMAX Application. International Journal of Advanced Research in Computer and Communication Engineering
Vol. 2, Issue 7, July 2013
5.P. KALPANA DEVI1, R. S. BHUVANESHWARAN worked on FPGA implementation of coefficient decimated polyphase filter bank structure for multistandard communication receiver. Journal of Theoretical and Applied Information Technology
20th June 2014. Vol. 64 No.2

III METHODES USED

Interpolation
Interpolation is a process of increasing the sampling rate and the device which performs it is called interpolator. The purpose of the interpolation is to get a new sequence with higher sampling rate without losing the information. Interpolation is a two-stage process, in first stage, the input signal is upsampled and then this upsampled signal is filtered. In the first stage, L-1 zero-valued samples are placed in between consecutive samples of the original

sequence, where L is the interpolation factor. Figure 1 shows the block diagram of the interpolator.

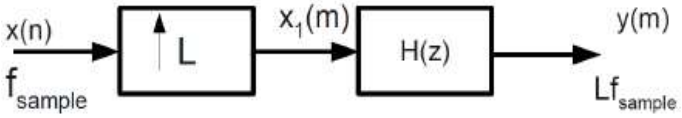

Figure 1. Interpolation by a factor of L.

2 Decimation

Decimation is the process of reducing the sampling rate and the device which performs this is called decimator. Decimation of a signal with a factor M is a two-stage process. The first stage is an anti-aliasing filter and second stage is a downsampler. By removing every Mth value of a signal, the sampling rate of the signal is reduced by a factor of M. This process is done by a downsampler. Figure 2 shows the block diagram of the decimator.

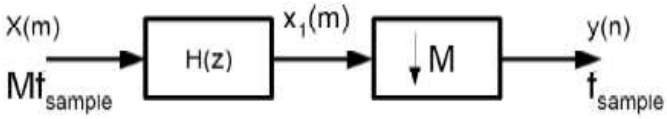

Figure 2. Decimation by a factor of M.

IV REFERENCES

1. Rajesh Mehra and Shaily Verma described FPGA Based Design of Direct Form FIR Polyphase Interpolator for Wireless Communication. International Journal of Electrical Electronics &Telecommunication Engineering, ISSN:2051-3240, Vol.44,Issue.1 1108

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