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COMPARISON OF 32-BIT RIPPLE CARRY ADDER AND CARRY LOOK-AHEAD ADDER IN VHDL

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Abstract- The paper describes the comparison between the 32-bit ripple carry adder (RCA) and 32-bit carry look-ahead adder (CLA). Adders are used in many data-processing systems to perform fast arithmetic operations. The ripple carry adder (RCA) gives the most compact design but takes longer computation time. The time critical applications use carry look-ahead adder (CLA) to derive fast result but least to increase in area. In this work we compared both adders on the basis of delay, power and area. This design has been synthesized by Spartan 3 family with XC3S400 device.

Keywords:- Adder, Ripple carry adder, Carry look-ahead adder, VHDL code

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INTRODUCTION

Adders are widely used in digital integrated circuits. High-speed adder is the necessary component in a data path e.g. Microprocessors and a Digital signal processor. For adding two binary numbers, there are several adder structures based on different design ideas. There are many binary adder architecture ideas to be implemented in such applications. The easiest type of parallel adder to build is a ripple carry adder, which uses a chain of one bit full adder to generate its output. The Ripple Carry Adder (RCA) gives the most compact design but takes longer computation time. The time critical applications use Carry Look-ahead scheme (CLA) to derive fast results but lead to increase in area. In mobile electronics, reducing area and power consumption are key factors in increasing portability and battery life. Even in servers and desktop computers, power consumption is an important design constraint. Design of area and power-efficient high-speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. Adders are extensively used in processing units such as the ALU's (Arithmetic Logic Unit) or in DSP (Digital Signal Processing) applications. A two-operand adder is used not only when performing additions and subtractions, but also often employed when executing more complex operations like multiplication and division. Consequently, a fast and area efficient two- operand adder is essential [3].

o   **Adders-**

A two-operand adder is used not only when performing additions and subtractions, but also often employed when executing more complex operations like multiplication and division. Consequently, a fast and area efficient two- operand adder is essential. Two basic kinds of adders are: Half-Adder and Full-Adder. A Half-adder is an adder that accepts two inputs and gives two outputs. A half adder consists of two logic gates. These are an AND gate, and an Exclusive OR gate. Full-adder performs the arithmetic sum of three bits. It consists of three inputs and two outputs. Three inputs involves two input bits plus an extra bit for an incoming carry. This is important for cascading adders together to create N-bit adders. A Full-Adder is made up of two Half-Adders and an OR gate. To add multiple inputs various types of Carry- Propagate Adders (CPA) are present. Among them RCA design occupies the small area but takes longer computing time. The delay of RCA is linearly proportional to number of input bits. For some input signals carry has to ripple all the way from least significant bit (LSB) to most significant bit (MSB). The propagation delay of such a circuit is defined as the worst case delay over all possible input patterns also called as critical path delay. The CLA offers a way to eliminate the ripple effect. For every bit, sum and carry is independent of the previous bits. CLA is faster than RCA but consumes large area. CLA is fast for a design having less input bits, for higher number bits it shows the worse delay [3].

▪   **Half-Adder -**

A Half-Adder is an adder that accepts two inputs and gives two outputs. The two inputs are the two single bit binary values. The two outputs represent the sum and carry. A half adder consists of two logic gates, an AND gate, and an Exclusive OR gate. A diagram of half adder shown below in Fig. 1. It has a two input A and B and two output Sum and Carry [3].
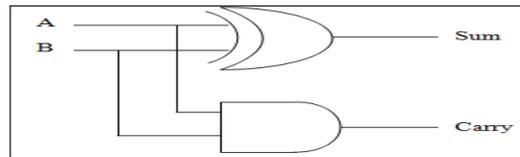
Fig. 1: Half Adder [3].

Full-adder -

The main difference between a Half-Adder and a Full-Adder is that a Full-Adder performs the arithmetic sum of three bits. It consists of three inputs and two outputs .Three inputs involve two input bits A and B plus an extra bit for an incoming carry Cin. Two outputs are Sum and carry out Cout. This is important for cascading adders together to create N-bit adders. A Full-Adder is made up of two Half-Adders and an OR gate. A diagram of Full adder shown in Fig. 2 [3].
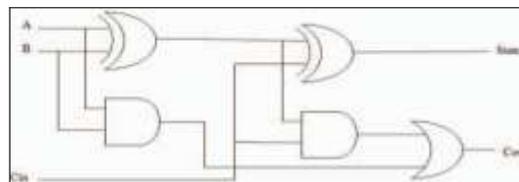

Fig. 2: Full Adder [3].

The most straightforward implementation of a parallel adder for two operands A_{n-1}, A_{n-2} . . . ,A_0 and B_{n-1}, B_{n-2}.....,B_0 is through the use of N basic full adders units. The FA is a combinational digital circuit implementing the binary addition of three bits [3].

A. **Ripple carry adder-**

Figure 3 depicts an 8-bit RCA, which is formed by a cascade of full adder modules. The full adder is an arithmetic building block that adds an augend and addend bit (say, a_0 and b_0) along with any carry input (Carry_in) and produces two outputs, namely, sum (Sum) and carry overflow (Carry_out). Since there is a rippling of carry from one full adder stage to another, the propagation delay of the RCA varies linearly in proportion to the adder width. This is called a RCA, since the carry signal "ripple" from the least significant bit position to the most significant bit position. The carry of this adder traverses longest path called worst case delay path through N stages [1].
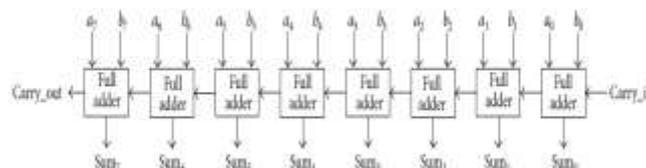

Fig. 3: 8-bit RCA [1].

B. **Carry look-ahead adder-**

It is well known that a CLA is faster than a RCA. Although the concept of carry look-ahead is widely understood, the concept of section-carry based carry look-ahead may not be that well known, and hence to explain the distinction between the two, sample 4-bit look-ahead logic realized using these two approaches is portrayed in Fig. 4 for an illustration [1].
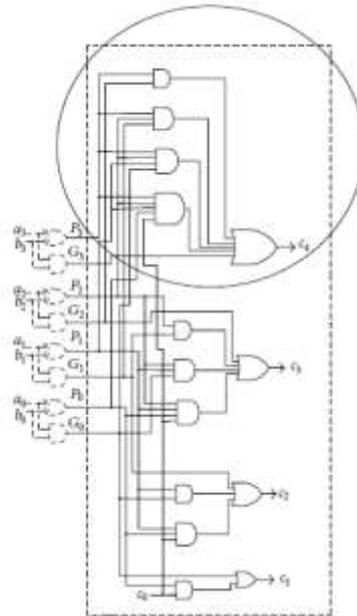
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Fig. 4: CLA [1]

The section-carry based carry look-ahead generator shown enclosed within the circle in Fig. 4 produces a single look-ahead carry signal corresponding to a "section" or "group" of the adder inputs (hence the term "section-carry"), while the conventional carry look-ahead generator encapsulated within the rectangle produces multiple look-ahead carry signals corresponding to each pair of augends and addend primary inputs. The section-carry based carry look-ahead generator differs from the traditional carry look-ahead generator in that bit-wise look-ahead carry signals are not required to be computed for the former [1].

The XOR and AND gates used for producing the necessary propagate and generate signals (P3 to P0 and G3 to G0) are highlighted using dotted lines in Fig. 4. We can calculate the generate bit, propagate bit, sum and carry in carry look-ahead generator form following equations [1].

$$C_4 = G_i + P_i + C_i$$
$$G_i = a_i + b_i$$
$$P_i = a_i \oplus b_i$$
$$SUM_i = P_i \oplus C_i$$

Where, G is a generate bit and P is a propagate bit. And symbol $\oplus$ is exclusive-or operation (XOR).

II. synthesis

The complete Design is modeled in Pure VHDL. The syntax of the RTL design is checked using Xilinx tool. For functional verification, the design is modeled in Hardware descriptive language (HDL). Test cases for the block level are generated in VHDL by both directed and random way.

The complete design along with all timing constraints, area utilization and optimization options are described using synthesis report. The adder design is synthesized at Spartan-3 (XC3S400).

III. RESULTS AND DISCUSSION

The output waveform of 32-bit RCA and CLA is given below in Fig. 5 and 6. The output waveforms are obtained using VHDL test bench.
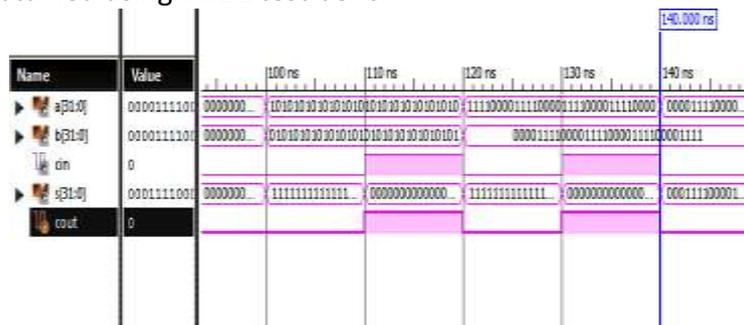

Fig. 5: Waveform of 32-bit Ripple Carry Adder

Fig. 6: Waveform of 32-bit Carry look-ahead Adder

The comparison of 32-bit Ripple carry adder and Carry look-ahead adder is shown in Table 1 and 2.

Table 1- Comparison of delay and power.

Adder	Delay(ns)	Power(mw)
RCA 32-bit	51.02	59.84
CLA 32-bit	50.94	59.84

Table 2- Area utilization of RCA and CLA.

Utilization summary	RCA 32-bit	CLA 32-bit
No. of slices Out of 3584	37	37

No. of 4 i/p LUT's Out of 7168	64	64
No. of bonded IOB's Out of 141	98	98

IV. CONCLUSION

The paper describes the comparison between the 32-bit ripple carry adder (RCA) and 32-bit carry look-ahead adder (CLA). The ripple carry adder (RCA) gives the most compact design but takes longer computation time. The time critical applications use carry look-ahead adder (CLA) to derive fast result but least to increase in area. In this work we compared both adders on the basis of delay, power and area.

Comparison of 32-bit RCA and CLA clearly indicates that there is no significant speed advantage of CLA over RCA at 32-bit or as number of bits are greater than 32-bit.

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