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VLSI BASED NETWORK ON CHIP 2X2 MESH TOPOLOGY

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Abstract- NoC is efficient on-chip communication architecture for soc architecture. In System on Chip the performance of the system has been sluggish due to the restriction of the common bus architecture espoused by these systems and thereby low processing speeds. In this paper, we proposed a implementation of a NoC for FPGA using Mesh topology. For efficient NoC architecture router should be efficient. We design here a router having four input and four output for Mesh topology. For packets routing from source router to the destination router XY routing algorithm is used. And our approach presents a supple design using FPGA based system. Hence it is very flexible network design that will accommodate to various needs. And finally verification is done on two different FPGA using Xilinx 13.1 software and we analyze the performance.

Keywords:- FSM Controller, Mesh Topology, NoC, XY routing Algorithm.

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INTRODUCTION

In old era ICs have been designed with dedicated point to point connections, with one wire dedicated to each signal. Due to this, large design had some limitations from physical design viewpoint. The wires (wire bus) occupy large area of chip and in CMOS technology, interconnection dominates performance and dynamic power dissipation. Network on Chip (NoC) is a new paradigm to make the interconnections inside a System on Chip (SoC) system. It reduces complexity of designing wires and also increases speed and reliability. NoC can provide separation between computation and communication supports modularity and IP reuse via standard
interfaces, serve as a platform for system test, handles synchronization issue, and, hence increasing engineering productivity. In NoC technology the bus structure is replaced with a network which is a lot similar to the Internet.
Segments communicate with each other by sending packetized data over this network. Network on Chip gives solution that the inter process communication among different modules takes place by transfer of packets instead of polling or arbitration as in bus architecture. The NOC design paradigm has been proposed as the future of ASIC design.
NoC is generally composed of three basic components: network interface (NIs), routers and resources. Router which is an element of the NoC topology, implements routing function, switching technique and the flow control algorithms. Topology of NoC defines the connectivity or the routing possibilities between nodes, thus having a fundamental impact on the network performance as well as the structure. The tradeoff between generality and customization becomes then an important issue when choosing a network topology.
For connecting cores to each other, there are many NoC topologies such as Mesh and Ring, Spidergon. To evaluate the NoC topologies, a simulation based approach was used for the modeling and analysis of the topologies. However, some properties of the topologies could affect the performance of the NoC systems. Among many topologies in massively parallel computer systems including the NoC architectures, interconnection networks have become the center of focus because of those network structures and topologies as well as the processing elements greatly influencing system cost and performance. We designed the 2x2 Mesh topology using XY routing algorithm and analyze its performance on different FPGA kit.

In section II, some related work is discussed. In section III, the overview of NoC design approach is introduced, in section IV, the detailed implementation of 2x2 Mesh topology is explained .section IV presents the Synthesis and simulation results of our design and In section V conclusions are discussed.

II. RELATED WORK

The 2x2 Mesh topology we design in this paper with efficient router which is avoiding congestion and communication bottleneck and XY routing algorithm which is live-locks free. Although there are various researches has already been done regarding various topology, some of the related works are included here. In [1], FPGA implementation of network on chip framework is given. In this they conclude that as compare to common bus architecture NoC architecture is effective in terms of speed performance and throughput. In [2] analysis

of five port router is given. The diagonal Mesh topology is designed to offer a good tradeoff between hardware cost and theoretical quality of service in [3]. In [4] they proposed efficient router architecture and support junction based routing in NoC platforms and analyse that Mesh topology is the most popular topology for NoC because it is suitable for two dimensional layouts and is structured and scalable. It is also easier to analyze and design efficient routing algorithms for mesh topology as compared to other topologies. Design can contain large number of nodes without changing the maximum diameter. They also present a new router architecture called Flexible, Extensible Router NoC (FeRoNoc). In [5], NoC is implemented using Torus topology. They proposed router architecture, a router algorithm and also provided solution to the problem introduced by the long wires in torus topology by pipelining both the long wires and short wires and by lengthening the input buffers attached to the long wires. Pratiksha Gehlot and Shailesh Singh Chouhan had evaluated performance of different Noc architectures and compare them on the basis of some performance parameter. They conclude that Mesh and Folded Torus has moderate values of all parameters [6]. In [7], they mainly worked on analysis of router. They discussed different types of router structure and used Markov chain analysis to derive an analytical model for input queue mesh based router. In [8], a low area overhead packet-switched NoC architecture is presented but the drawback with that is , packet has two headers which is quite expensive. The buffer here is present only with input channel. The absence of output buffer creates a serious problem in the implementation of router as it increases the problem of congestion.

II. AN OVERVIEW OF NOC DESIGN APPROACH

Switching method, Topology and Routing algorithm are three important things in the design of NoC.

A. Switching Technique:

Circuit switching and packet switching are two major switching techniques. Packet switching is better than circuit switching as it does not reserve the path like circuit switching. Packet switching is utilized in most of NoC platforms because of its potential for providing simultaneous data communication between many source-destination pairs. Further it can be classified into Store and forward, Virtual cut through and Wormhole switching [10].

B. Topology:

Topology defines how nodes are placed and connected, affecting bandwidth and latency of a network. Many different topologies have been proposed [5] [6]. Such as mesh, torus, octagon, SPIN etc. Some researchers have proposed application specific topology that can offer superior performance while minimizing area and energy consumption. Most common topology is 2-D Mesh due to its grid-type shapes and regular structure which are the most appropriate for the two dimensional layout on a chip. Mesh topology is easy to implement as all nodes are equally distance as shown in Figure.1 and also makes addressing of the cores quiet simple during routing. The local interconnection between the resources and routers are independent of the size of network. Moreover routing in a 2-D Mesh is easy resulting in potentially small switches, high capacity, short clock cycle and overall scalability [11]. Therefore we choose the mesh topology. A mesh topology has four inputs and four

outputs from/to other routers, and another input and output from/ to the PE. So we design here router for the implementation of mesh topology.

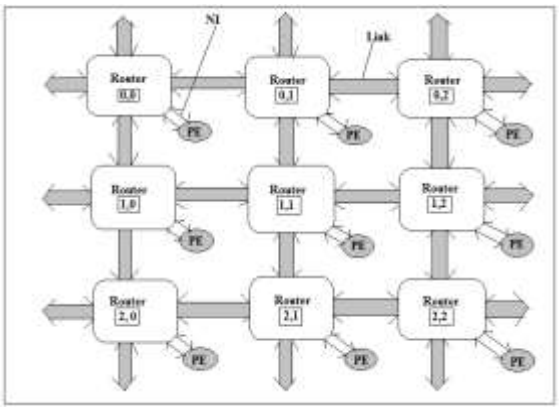

Figure 1: 3x3 Mesh Topology

C. Routing Algorithm:

The routing algorithm which defines a path taken by a packet between the source and the destination is a main task in network layer design of NoC[12]. According to how a path is defined to transmit packets, routing can be classified as deterministic or adaptive. In deterministic routing, the path is uniquely defined by the source and target addresses. Deterministic routing algorithms are widely used due to easy implementation. and in adaptive routing algorithm use information about the network's state to make routing decisions. A mesh network topology consists of m column and n rows. The routers are situated in the interconnection of two wires and processing element near routers. Addresses of routers and resources can be easily defined by X and Y co-ordinates in a mesh. Hence for Mesh topology XY deterministic routing algorithm is used.

III. DESIGN OF 2x2 MESH TOPOLOGY

For the implemplementation 2x2 Mesh topology shown in figure 2, we required the efficient router architecture and suitable routing algorithm which we designed in this paper.

A. ROUTER ARCHITECTURE

A router is a device that forwards data packets across computer networks. A router is a microprocessor controlled

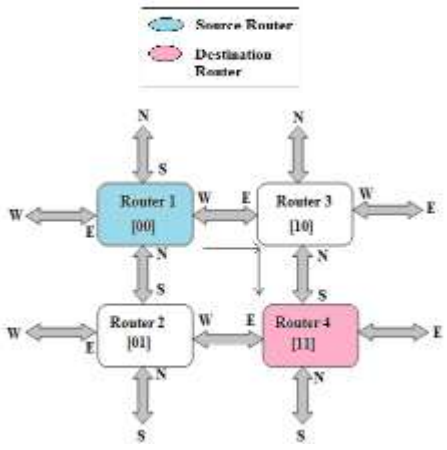

Figure 2: 2X2 Mesh Topology with Router Address showing Routing Path

device that is connected to two or more data lines from different networks. When a data packet comes from in on one of the lines, the router reads the address information in the packet to determine its ultimate destination. With the help of routing algorithm it directs the packet from router to router through the networks until it goes to the destination.

The 1x4 router block consist of four blocks i.e. register, demultiplexer, FIFO, controller. The register is similar to the buffer which stores the input data. Demultiplexer provides the channel which sends the input data to the appropriate output port. FIFO is a first in first out memory queue with control logic that manages read and write operations. It is used to control the flow of data between source and destination. The controller is based on FSM deterministic routing which improves the performance of router. The router which we design is a four port network router. Router accepts the data in the form of packet. Packet width is 8 bits having last 2 bits as the port address and remaining bits are data bits. The router drives the packet to respective ports based on the destination address of the packets. Figure 3 shows the block diagram of the 1x4 router block. This block is used in the design of the central router of Mesh topology having four input and four output ports shown in Figure.4, In this block transfer of data from all inputs to all output ports is carried out by round robin mode.

1. Register:

We design the 8 bit register having clock, reset and enable. At the posedge of the clock, reset should be low and enable should be high then and only then we get the output. When enable remain low, the register keeps its current value. The output of the register is the input of the demultiplexer. The register is acting as a buffer. It stores the value temporally. As the register we design here, it first stores the data and forwards it when all the conditions are proper. We use the store and forward flow control which avoid the congestion.

2. *Demultiplexer* :

We design the 1:4 bit demultiplexer to define the four output ports. The last two bits of the input data acts as a select signal which indicates the port. Table I Shows the output port

regarding last two bits. Demultiplexer transfers the data coming from the register block to the appropriate output port

TABLE I: Port identification

Sr. No.	Last Two Bits of Data	Output Port
1.	00	Port 1
2.	01	Port 2
3.	10	Port 3
4.	11	Port 4

According to the last two bits define in the table. The demultiplexer also has an enable. When enable is high then only the demultiplexer directs the data to the appropriate output port at the same time corresponding write enable pin should also high. And other output ports and write enable pin should remain zero. The output of the each port is connected to the individual FIFO unit.

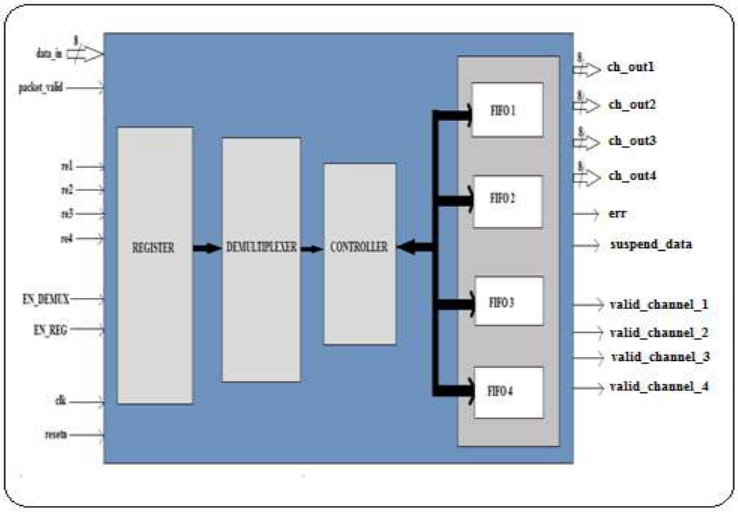

Figure 3: Internal Structure of Router Block

3. FIFO

We design the FIFO block having 8 bit width and memory array of 0 to 15 location which stores the data called as depth of memory array. Here there are four fifo's to store the data coming from individual output ports,It performs the read and write operations. Fifo have fifo_full and fifo_empty control signals. Fifo's are used to safely pass multi-bit data words from one clock domain to another or to control the flow of data between source and destination side sitting in the same domain. Here for read and write operation we use the synchrounous clock. Write operation is done at the posedge of the clock when the reset is low, write enable pin is one and fifo is not full. In this condition only the data write into the memory of the fifo. Read operation is done at the rising edge of the clock ,when reset is low

and simultaneouly the read enable pin also one and fifo is not empty then only the data is read from the memory of the fifo.

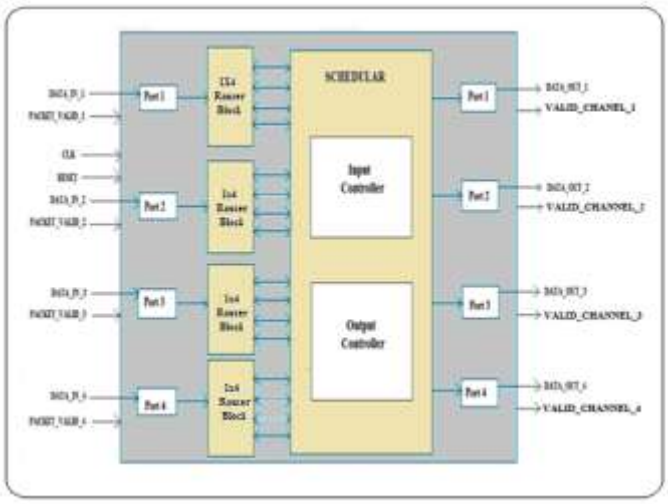

Figure 4: Internal structure of MESH Router

When the fifo_full signal is high, it indicates that all the locations inside the fifo has been written and it is unable to write the data into the memory of fifo. Similarly when the fifo_empty signal is high, it indicates that all the locations inside the fifo has been empty and it is unable to read the data from the memory of the fifo. For four fifo blocks there are four fifo_full signals and fifo_empty signals which is the input to the controller.

4. FSM Controller:

This module generates all the control signals when new packet is coming to the router. These control signals are used by other modules to send data at output. As the demultiplexers output is connected to the contoller, the data of the each port is accepted by the controller when the respective port enable pin is high as well as packet_valid signal is high. At the posedge of the clock when resetn is low then only data can be accepted. fifo_full and fifo_empty signals are also handlled by the controller. There are four FIFO's regarding four output ports.Controller checks which fifo is full, which FIFO is empty and according to the port address it gives signal to write the data into the respective FIFO when we pin of controller is high. and when fifo_full signal becomes high data is read from the respective FIFO and send to the respective output port of the controller. When reading process is completed data is ready to transmit. It indicates by the respective valid_chanel signal when it becomes high. There are four valid_chanel for the four output ports of the controller. if any one of the chanel is low, it means that chanel is busy in communicating and respective fifo_empty signal is high. It means that it is ready to write the data into the present fifo. When the suspend_data signal is low, then only router can accept the new data from the input and latched data is send to the FIFO and we pin is generated for writing the data into present FIFO. In present controller, fsm logic is used due to which cycle for each output port is repeated. Hence performance is increases.

B. XY ROUTING ALGORITHM

For the implementation of 2x2 Mesh topology, we require the routing algorithm to route the packets from one router to other router still destination router is not meet. There are different routing algorithms. But XY routing algorithm is suitable for the 2 dimensional mesh topology. A deterministic XY dimension-ordered routing algorithm, also a shortest path algorithm, is implemented and operates by first routing packets along the x-direction until they reach the x-destination address and then likewise for the y-dimension. This means that packets always traverse the same path between a particular set of source-destination nodes. The deterministic algorithms usually have less computation and are able to find the next hop in a shorter time. The deterministic algorithms are mostly based on indexes and therefore are more suitable in NOCs which have predetermined structures. These algorithms are used in both regular and irregular networks. Because of the simplified logic, the deterministic routing provides low routing latency and good reliability when the network is not congested. These algorithms suffer from low tolerance against the possible faults in the networks and thus as the packet injection rate increases, they provide throughput and efficiency degradation as they cannot dynamically respond to network congestion.

On the other hand adaptive algorithms often need more computations and in order to select the correct path they need some information about the current state of the network. The adaptive algorithms simultaneously perform the routing and packet forwarding. After each hop they select the next hop according to the current state of the nodes and links traffic. Thus there is always a possibility of live lock occurrence in them. But one of the advantages of deterministic XY routing over adaptive routing is that it never runs into deadlock or live-lock.

IV. SYNTHESIS AND SIMULATION RESULT

A. Synthesis :

The synthesis of the proposed design has been done using Xilinx. Figure 5 is the RTL schematic of 2x2 Mesh topology using XY routing algorithm to route the packet from source router to destination router.

B. Simulation Result :

Simulation refers to the verification of a design, its function and performance.The simulation is performed in Xilinx 13.1 software. Figure 6 shows the simulation result of the 2x2 Mesh topology. In 2x2 Mesh topology at the posedge of clock, when reset is low, the incoming packet is transferred from any one port of source router to any one port destination router according to source and destination addres of the router as well as port addres of both router defined in the packet. As we are using XY routing algorithm to route the packet, first the packet goes to X direction and then Y direction untill destination is not reached. It is indicate that packet is reached from source router to the particular port of the destination router making particular valid channel signal high which is shown in figure 6 and sythesis details of Mesh topology on two different FPGA is given in TABLE II.

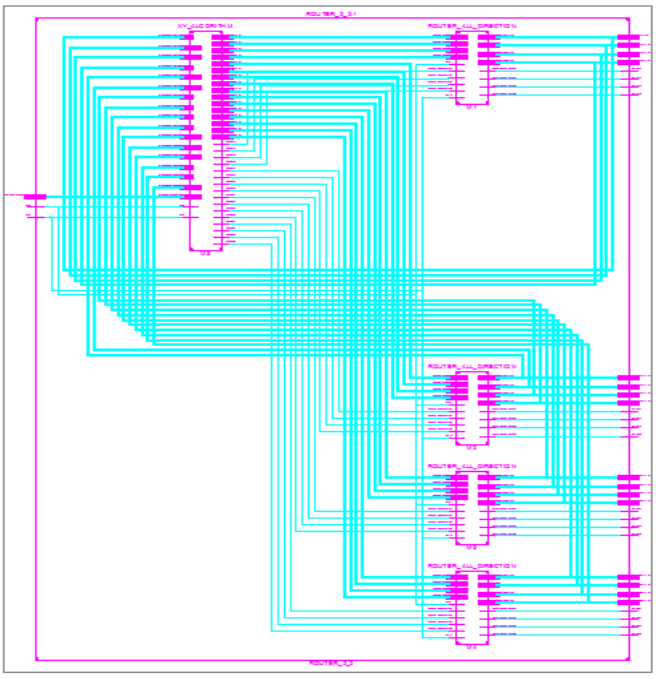

Figure 5: RTL Schematic of 2x2 Mesh topology using XY routing algorithm

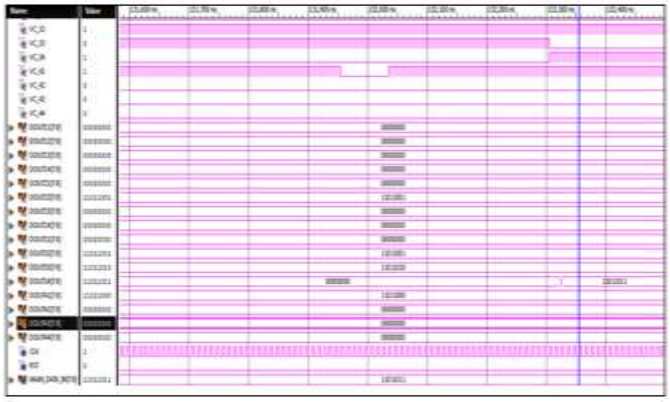

Figure 6: Simulation Result of 2x2 Mesh Topology using XY routing algorithm

TABLE II: Synthesis Details of Mesh Topology

Sr. No.	Parameters	Mesh Topology on SPARTEN6 (xc6slx16-3csg324)	Proposed design on VERTEX 6 (xc6vlx240t-1ff1156)
1	Delay	11.697 ns	7.237 ns
2	Frequency	85.493 MHz	138.187 MHz
3	Memory	256 MB	267.664 MB
4	On chip Power	0.0359W	0.07991W

V. CONCLUSION AND FUTURE SCOPE

A network on chip is a valid approach to meet the communication requirements in system on chip. In network on chip interconnections are realized using network. We implement the 2x2 Mesh topology using deterministic XY routing algorithm. In this thesis, we also analyze the performance parameters like frequency, delay, memory and on chip power by synthesizing our design on different FPGA. It is found that delay of our design is less in Vertex 6 FPGA compared to Spartan 6. As we require the network should be fast means any data can be reached to its destination as early as possible, therefore we can say that Vertex6 is more suitable than Sparten6. We have implemented only one topology i.e. Mesh topology. In future we can work on various topologies and its implementation on FPGA. Also we can work on application based on the Topologies.

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