INTERNATIONAL JOURNAL OF PURE AND APPLIED RESEARCH IN ENGINEERING AND TECHNOLOGY

A PATH FOR HORIZING YOUR INNOVATIVE WORK

DESIGN AND IMPLEMENTATION OF LOW POWER TERNARY DECODER

V. S. INGOLE, V. T. INGOLE

Department of Electrical Engineering, G. H. Raisoni College of Engineering, Nagpur, India.

Accepted Date: 15/03/2016; Published Date: 01/05/2016

Abstract: Design of Ternary logic circuit is inherently more challenging than its Binary counterpart. Due to its popular nature, all semiconductor devices have been designed and fabricated to suit Binary logic. Many challenges are faced while developing the different multivalued circuits. In the present paper implementation of the Low power Ternary Decoder with fewer numbers of CMOS devices is presented. Decoder is the basic building block of different Ternary logic gates like TNAND, TXOR and THALF ADDER and TERNARY FULL ADDER. Simulation result shows encouraging output results.

Keywords: Low Power, Design, Implementation

Corresponding Author: MS. V. S. INGOLE

Access Online On:

www.ijpret.com

How to Cite This Article:

V. S. Ingole, IJPRET, 2016; Volume 4 (9): 15-20

PAPER-QR CODE

1. INTRODUCTION

There is a remarkable rise in the requirement for low power devices and smaller chip area. In normal VLSI circuit the area requirement is generally large due to large number of interconnection. It has been established and reported [8] that in Ternary logic such interconnections are greatly reduced due to higher logic states. Many Ternary circuit implementations have been reported [7] however the device count is large. There appears to be a need of fewer device count chip with low power consumption for its successful implementation in ALU [5].

2. TERNARY LOGIC

The logic level defined in Ternary is in three different reference voltages 0 ,Vdd/2 and Vdd. Binary design used two states “true” or “false”, Ternary logic has three states, “true”, “false” and “unknown”[3]. These voltage levels are shown in fig 1 and fig 2 respectively [10].

3. TERNARY LOGIC GATES

3.1PTI (Positive Ternary inverter)

The proposed PTI is composed of only one p channel and N channel MOSFET by adjusting Length and width ratio[4]. The proposed PTI is having L/W ratio of 15us/1um. The source of PMOS and NMOS is connected to the supply voltage VDD and ground. The power dissipation of the proposed design is low as compared to conventional design**[**1][7].

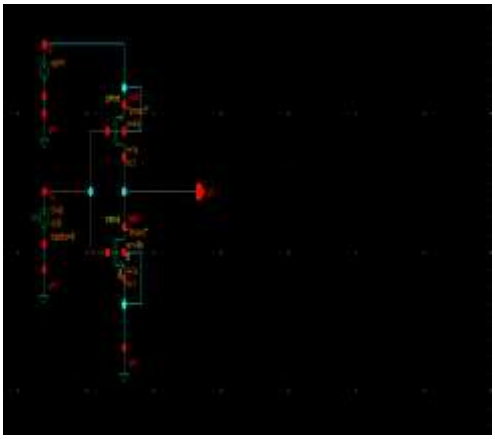

Figure 1:Schematic of PTI

3.2NTI (Negative Ternary inverter)

The proposed NTI is composed of one p channel and N channel MOSFET by adjusting Length and width ratio. The proposed NTI is having L/W ratio of 1us/6um. The source of PMOS and NMOS is connected to the supply voltage VDD and ground[9]. The power dissipation of the proposed design is low as compared to conventional design and number of gate is reduced**[1][4].**

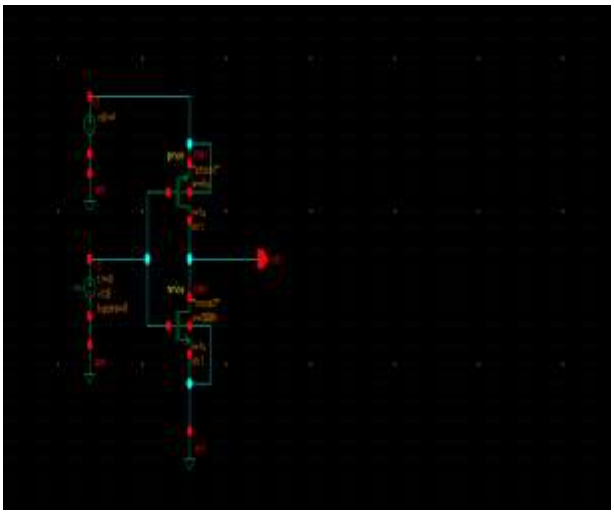

Figure 2: Schematic of NTI

4. DECODER

We have given a single input to the proposed decoder design and taking three outputs from it namely Y0, Y1, Y2 respectively. This proposed decoder circuit is composed of Positive Ternary Inverter, Negative Ternary Inverter and NOR gate .Input logic to decoder is 0, 1, 2 (X) which is given to the PTI and NTI simultaneously. The output of PTI and inverted output of NTI is given to the NOR gate to get the output for an intermediate state. The first and third state of decoder is taken from the inverted output of PTI and output of NTI respectively. The output of decoder is Y0, Y1, and Y2 as a function of X which is shown in figure. This decoder circuits consists of only 10 transistors[2].

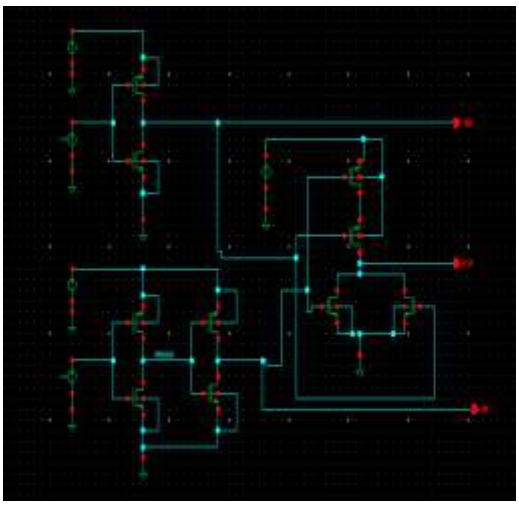

Figure 3: Schematic of Decoder

5. SCHEMATIC & RESULT:

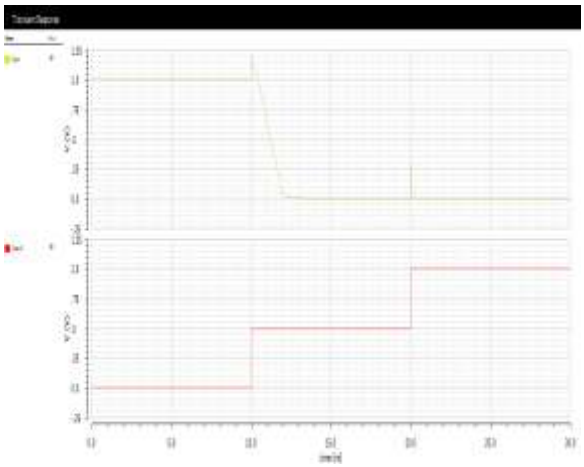

Figure: 4 Output of PTI

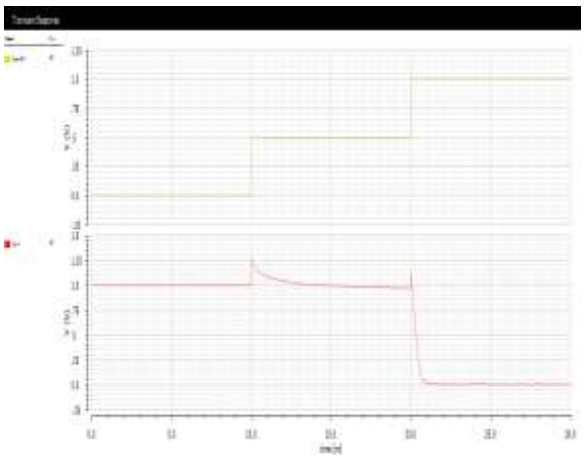

Figure 5: Output of NTI

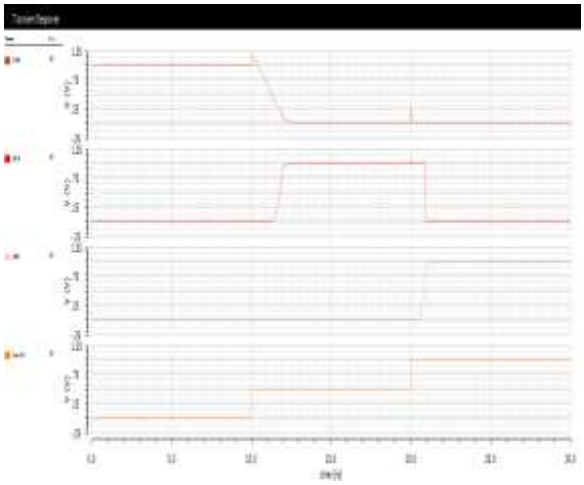

Figure 6: Output of Decoder

Table: Power Consumption

	Proposed Design	
	Power Dissipation	**No. of gates Required**
PTI	1×10^{-10}w	**2**
NTI	1×10^{-10}w	**2**
Decoder	5×10^{-10}w	**10**

5. CONCLUSION:

A complete design of ternary decoder is explained.proposed design og gates is design very simple with few number of gates.this decoder design can be used as a different combinational design.

6. REFERENCE:

1. Design and implementation of 2 bit Ternary ALU slice A. P. Dhande V. T. Ingole,3rd international conference: sciences of electronic, Technologies of information and telecommunications March 17-21, 2005 – Tunisia.
2. "Depletion/enhancement CMOS for a low power family of three-valued logic circuits" Alex Heung and H. T. Mouftah, senior member, IEEE journal of solid-state circuits, vol sc-20, no 2, April 1985.
3. "Design of Ternary CMOS memory and sequential circuits"IEEE trans. Computers, vol. C-26, pp. 281 –288, mar. 1977.
4. "Implementation of combinational circuits using Ternary multiplexer" Shweta Giri, Mrs.N.Saraswathi, International journal of computational engineering research / ISSN: 2250–3005.
5. "A new CMOS Ternary logic design for low-power low-voltage circuit", Mariani, F. Pessolano, R. Saletti.
6. "A framework for design of multivalued logic functions and its application" Mudhafar A.Hassan Ali, student member, Zeee, Falah J. Hassan-Alshiroofi and Hemant G. Rotithor, senior member, IEEE.
7. Design of 3-valued r-s & d flip – flops based on simple Ternary gates Using CMOS Ternary switches, A.P.Dhande and V.T.Ingole, proceedings of world academy of science, engineering and technology volume 4 February 2005 ISSN 1307-6884.
8. VLSI Design and Implementation of Ternary Logic Gates and Ternary SRAM cell, Ms. Nilmani P. Wanjari, Ms. Shweta P. Hajare international journal of electronics and computer science engineering.
9. CMOS Ternary logic circuits X.W. WU Prof. F.P. Prosser, PhD IEE Proceedings, vol. 137, pt. G, no. I, February 1990.
10. "A brief introduction to Ternary logic"Jorge Pedraza Arpasi, 7th November 2003.