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SEPIC MULTIPLIED BOOST CONVERTER ANALYSIS AND SIMULATION

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Abstract: - This paper analysis a switched mode power supply topology which is a variation of SEPIC (single ended primary inductance converter). It is called SEPIC multiplied boost converter (SMBC) and is analyzed using volt second and charge balance across inductors and capacitors respectively. Equations derived are validated through simulations. It also derives averaged state space equations for small signal analysis. This is necessary for understanding the frequency response of the power stage. It helps to design controller based on the gain margin and phase margin available through this model. This paper considers ideal switch for basic insight into this topology.

Keywords: Switched mode power supply, SEPIC Multiplied boost

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INTRODUCTION

This document is based on the novel and tested topology for boost converters with moderately high boost ratios[1].This application note describes the advantages offered by the topology called SEPIC multiplied boost(SMBC) converter over other available topologies to boost voltage. SMBC is capable of stepping up voltage to very high levels from low input voltage level with.

This application note[1] lists following benefits of this topology:

•Reduction in voltage stress on the main and rectifier switches widening and improving the choices in MOSFETs and Schottky rectifiers, for which high voltage is often a disadvantage.

• Reduced pulse-width modulation (PWM) duty cycles that allow continuous conduction mode (CCM) operation.

• Better efficiency due to: moderate duty cycles, lower voltage MOSFETs and rectifiers, and reduced switching losses due to reduced peak-to-peak voltage swing.

• Reduced noise due to reduced energy in switch node capacitance. In addition, high frequency emissions may be reduced because multiple inductor energy discharge paths seem to dampen high frequency ringing.

A SMBC can have higher number of stages for conversion ratio exceeding 10 times the input voltage. This paper analyzes single stage conversion in the converter. This paper also derives a model of the topology using averaged state space equations. However the parasitic values associated with each component in the topology are neglected for simplicity. This is a fifth order boost converter. Other topologies of boost converter of higher order are analyzed in [2] and [3]. DC-to-DC power converters are difficult to simulate in computer packages, such as Simnon, or MATLAB, when considered in their traditional physical circuit form equations. Numerical precision demands extremely small integration steps[4]. Hence, modeling power converters reduces demands on computer processing capabilities. Disadvantages of SMBC are higher parts count and increased forward voltage drop due to series connected rectifiers.

Steady state circuit analysis

Modeling and analysis of certain topologies containing more than two storage elements was done in[5]. Steady state analysis of SMBC is carried out using inductor volt-second balance theorem and capacitor Ampere-second law. Inductor volt-second balance theorem states that for steady state operation of inductor in a DC-DC converter, total inductor voltage in a

switching period is zero. Capacitor Ampere-second law states that for steady state operation of a capacitor in a DC-DC converter, total capacitor current in a switching period is zero.

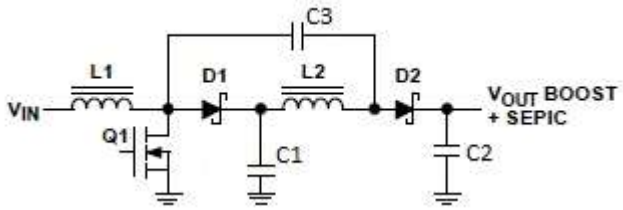

Fig. 1. SEPIC Multiplied Boost Converter with N =2[*1*]

Figure 1 shows a schematic of a single stage SMBC. Q1 is a MOSFET and acts as the main switch. D1 and D2 are switching diodes. L1 and L2 are primary and secondary inductors. Their inductances equal to L1 an L2 respectively. C1, C2 and C3 are called primary, secondary and coupling capacitors respectively. Their capacitances equal to C1, C2 and C3 respectively. The analysis follows following simplifying assumptions:

1) MOSFET and diodes are perfect switches having no voltage drops or losses in them.

2) Inductors and capacitors are of large values and have no parasitic resistances.

There are two states in the operation of this converter. These states are defined by switch operations. When switch Q1 is ON equivalent circuit of Figure 1 reduces to Figure 2. When switch Q1 is OFF equivalent circuit of Figure 1 reduces to Figure 3. Let i_1, i_2be the instantaneous current values in L1and L2 respectively and v_1, v_2, v_3 be the instantaneous voltages across C1, C2, C3 respectively

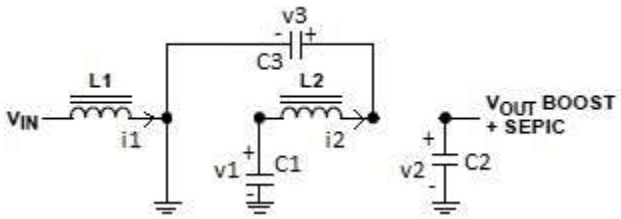

Fig. 2. Equivalent circuit of SMBC when Q1 is ON

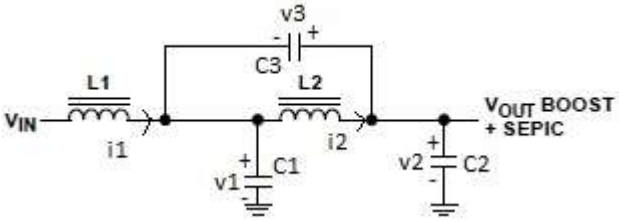

Fig. 3. Equivalent circuit of SMBC when Q1 is OFF

For linear ripple approximations, let $\langle v1\rangle = V_1;\ \langle v2\rangle = V_2;\ \langle v3\rangle = V_3;\ \langle i1\rangle = I_1;\ \langle i2\rangle = I_2$ and switching period be T_s.

Average voltage across L1 is given by:

$$\langle V_{L1}\rangle = DV_{in} + D'(V_{in} - V_1) = 0$$

Or

$$\mathrm{V_{in}} = \mathrm{D'V_1} \tag{1}$$

Average voltage across L1 is given by:

$$\langle V_{L2}\rangle = D(V_1 - V_3) + D'(V_1 - V_2) = 0$$

But

$$V_3 = V_2 - V_1$$

Hence output voltage is given by

$$\mathrm{V_{out}} = \mathrm{V_2} = (1 + \mathrm{D})\mathrm{V_1} \tag{2}$$

Combining (1) and (2), steady state voltage transfer function is given by

$$\mathrm{V_{out}} = \frac{(1 + \mathrm{D})\mathrm{V_{in}}}{\mathrm{D'}} \tag{3}$$

Charge gained by C1 when Q1 is OFF is $\mathrm{D'I_1(from\ L1)} - \mathrm{D'I_2(continuous\ charge\ loss\ through\ L2)} - \mathrm{DI_{L2}}$(charge drawn by C3). Charge lost by C1 when Q1 is ON is given by, $\mathrm{DI_2}$. Equating lost and gained charges,

$$\mathrm{I_2} = \frac{\mathrm{D'I_1}}{(1 + \mathrm{D})} \tag{4}$$

Similarly, applying charge balance across C2 we get output current

$$\mathrm{I_0} = \mathrm{I_2} \tag{5}$$

Steady state voltages and currents are independent of inductance and capacitance values. But the waveform ripples are characterized by the passive component values of capacitances and inductances. Peak to peak ripple calculations give:

$$\Delta i_1 = \frac{DT_s}{L_1} V_{in}$$

$$\Delta i_2 = \frac{DT_s}{L_2}(V_1 - V_3) = \frac{DT_s}{L_2} V_{in}$$

$$\Delta v_1 = \frac{DT_s}{C_1} I_2 = \frac{DT_s}{C_1} I_0$$

$$\Delta v_2 = \frac{DT_s}{C_2} I_0 \quad (6)$$

$$\Delta v_3 = \frac{DT_s}{C_3} I_2 = \frac{DT_s}{C_3} I_0$$

where $\Delta i_1, \Delta i_2, \Delta v_1, \Delta v_2, \Delta v_3$ are ripples in i_1, i_2, v_1, v_2, v_3 respectively.

Transistor peak inverse voltage is given by

$$\text{PIV(Transistor)} = V_1 + \Delta v_1/2 = \frac{V_{in}}{D'} + \frac{DT_s}{2C_1} I_0 \quad (7)$$

Transistor peak current is given by

$$PC(Transistor) = I_1 + \frac{\Delta i_1}{2} + I_2 + \frac{\Delta i_2}{2}$$

$$= \frac{(1+D)I_0}{D'} + \frac{DT_s}{2L_1} V_{in} + I_0 + \frac{DT_s}{2L_2} V_{in}$$

$$\text{PC(Transistor)} = \frac{2I_0}{D'} + \frac{DT_s}{2} V_{in} \left(\frac{1}{L_1} + \frac{1}{L_2}\right) \quad (8)$$

Diode D1 peak inverse voltage is given by

$$\text{PIV(Diode D1)} = V_1 + \frac{\Delta v_1}{2} = \frac{V_{in}}{D'} + \frac{DT_s}{2C_1} I_0 \quad (9)$$

Diode D2 peak inverse voltage is given by

$$PIV(Diode\ D2) = V_2 + \frac{\Delta v_2}{2} - V_3 + \frac{\Delta v_3}{2}$$

$$\mathrm{PIV(Diode\ D2)} = \frac{\mathrm{V_{in}}}{\mathrm{D'}} + \frac{\mathrm{DT_s}}{2}\mathrm{I_0}\left(\frac{1}{\mathrm{C_3}} + \frac{1}{\mathrm{C_2}}\right) \quad (9)$$

Peak currents through diodes D1 and D2 has been conditionally determined by following equations

When C3 << C2, $PC(Diode\ D2) = PC(Transistor)$

$$PC(Diode\ D1) = I_1 + \Delta i_1\left(\frac{1}{2} - \frac{DI_1}{D'^2 I_2}\right)$$

$$\mathrm{PC(Diode\ D1)} = \frac{(1+\mathrm{D})\mathrm{I_0}}{\mathrm{D'}} + \frac{\mathrm{DT_s}}{\mathrm{L_1}}\mathrm{V_{in}}\left(\frac{1}{2} - \frac{\mathrm{D}(1+\mathrm{D})}{\mathrm{D'^3}}\right) \quad (5)$$

However values of peak currents through diodes D1 and D2 for all possible values of capacitances need detailed analysis of exponential functions which is beyond the scope of this paper.

state space analysis

State space equations of SMBC can be found by averaging the state equations over the duty cycle. However, effects of fast switching are neglected in such a model[6]. Let resistance R be connected at the output. During ON period, state dynamic equations are found to be as follows.

$$\frac{\mathrm{di_1}}{\mathrm{dt}} = \frac{\mathrm{v_{in}}}{\mathrm{L_1}}$$

$$\frac{\mathrm{di_2}}{\mathrm{dt}} = \frac{(\mathrm{v_1} - \mathrm{v_3})}{\mathrm{L_2}}$$

$$\frac{\mathrm{dv_1}}{\mathrm{dt}} = -\frac{\mathrm{i_2}}{\mathrm{C_1}} \quad (3)$$

$$\frac{\mathrm{dv_3}}{\mathrm{dt}} = \frac{\mathrm{i_2}}{\mathrm{C_3}}$$

$$\frac{dv_2}{dt} = \frac{v_2}{RC_2}$$

During OFF period, state dynamic equations are found to be as follows:

$$\frac{di_1}{dt} = \frac{(v_{in} - v_1)}{L_1}$$

$$\frac{di_2}{dt} = \frac{(v_1 - v_2)}{L_2}$$

$$\frac{dv_1}{dt} = \frac{i_1(C_2 + C_3)}{\Delta} - \frac{i_2(C_2)}{\Delta} - \frac{v_2(C_3)}{\Delta R}$$

$$\frac{dv_2}{dt} = \frac{i_1(C_3)}{\Delta} + \frac{i_2(C_1)}{\Delta} - \frac{v_2(C_3 + C_1)}{\Delta R} \quad (4)$$

$$\frac{dv_3}{dt} = \frac{i_1(-C_2)}{\Delta} + \frac{i_2(C_1 + C_2)}{\Delta} - \frac{v_2(C_1)}{\Delta R}$$

Where

$$\Delta = \begin{vmatrix} (C_1 + C_3) & -C_3 \\ -C_3 & (C_2 + C_3) \end{vmatrix} = C_1C_2 + C_3(C_1 + C_2)$$

Taking average of dynamic equations over duty cycle d, we get state space representation as follows:

$$\dot{\boldsymbol{X}} = \boldsymbol{AX} + \boldsymbol{BU}$$

Where

$$\dot{\boldsymbol{X}} = \begin{bmatrix} \dot{i_1} \\ \dot{i_2} \\ \dot{v_1} \\ \dot{v_2} \\ \dot{v_3} \end{bmatrix}, \boldsymbol{X} = \begin{bmatrix} i_1 \\ i_2 \\ v_1 \\ v_2 \\ v_3 \end{bmatrix}, \boldsymbol{U} = v_{in}, \boldsymbol{B} = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

And A is given by

$$\begin{bmatrix} 0 & 0 & -\frac{1}{L_1}(1-d) & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & -\frac{(1-d)}{L_2} & -(d)\frac{1}{L_2} \\ \frac{C_2+C_3}{\Delta}(1-d) & -\frac{C_2}{\Delta}(1-d)-\frac{d}{C_1} & 0 & -\frac{C_3}{\Delta R}(1-d) & 0 \\ \frac{C_3}{\Delta}(1-d) & \frac{C_1}{\Delta}(1-d) & 0 & \frac{d}{RC_2}+\frac{(C_3+C_1)}{\Delta R}(1-d) & 0 \\ -\frac{C_2}{\Delta}(1-d) & \frac{C_1+C_2}{\Delta}(1-d)+\frac{d}{C_3} & 0 & \frac{(-C_1)}{\Delta R}(1-d) & 0 \end{bmatrix}$$

The above representation is a large signal representation of the converter and it needs to be linearized for applying small signal analysis for controller design of this topology as is done in[5] and [7].

Simulation results

In order to validate the steady state analysis, waveforms generated using LTSpice SPICE simulator was compared with the calculated results.

Specifications for the simulation are as follows:

V_{in} = 20 V; D = 0.805; R = 2160 Ohms

Comparison of calculated and simulated results is shown in table (1)

Table 1 Comparison of calculated and simulated values

Steady state values	Calculated Values	Simulated values
$\mathbf{V_1}$	102.5 V	103.5 V
$\mathbf{V_2}$	185.12 V	185.5 V
$\mathbf{I_1}$	793.34 mA	875.87 mA
$\mathbf{I_2}$	85.7 mA	85.657 mA
$\mathbf{\Delta i_1}$	16 mA	16 mA
$\mathbf{\Delta i_2}$	16 mA	16 mA

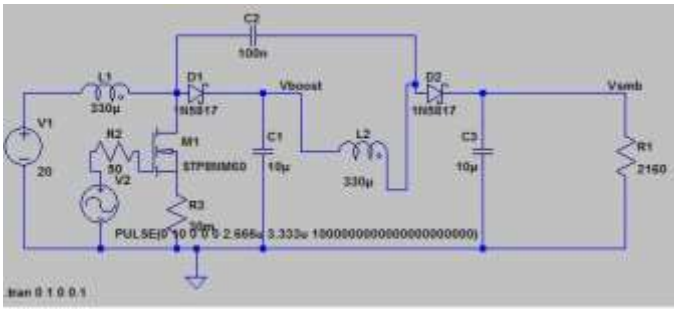

Figure 4 Schematic for simulation of SMBC

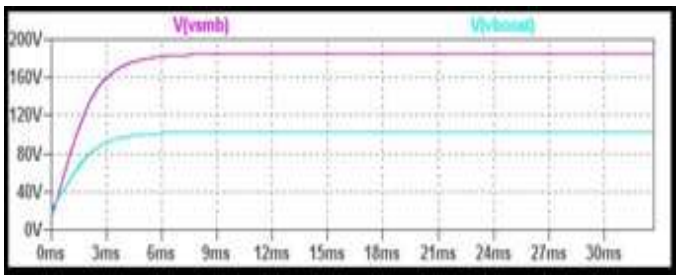

Figure 5 Voltage values at Vboost and Vsmb in schematic shown in fig. 4.

Values of I1 vary considerably due to power loss occurring in resistor and active components in the schematic.

Fig.5 and 6 indicate the voltage and current waveforms respectively.

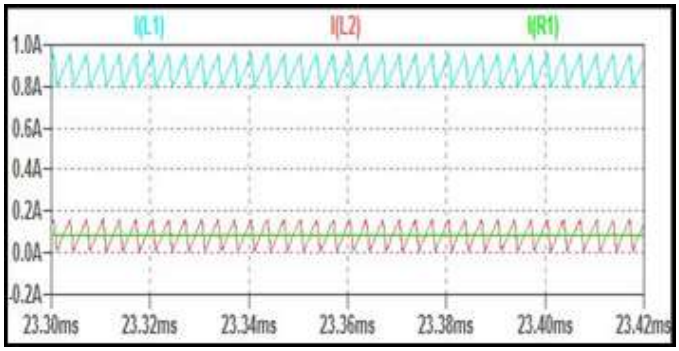

Figure 6 Currents through L1, L2 and output current

CONCLUSION

A dc–dc voltage converter has been studied and analyzed theoretically. Since dc shift in primary inductor is greater than secondary inductor, inductor of smaller air-gap can be used for secondary inductor. Capacitance of coupling capacitor controls the peak currents through the

series diodes making it a critical design parameter. However, small signal analysis of this converter is tedious approaches other than conventional method has to be deviced.

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